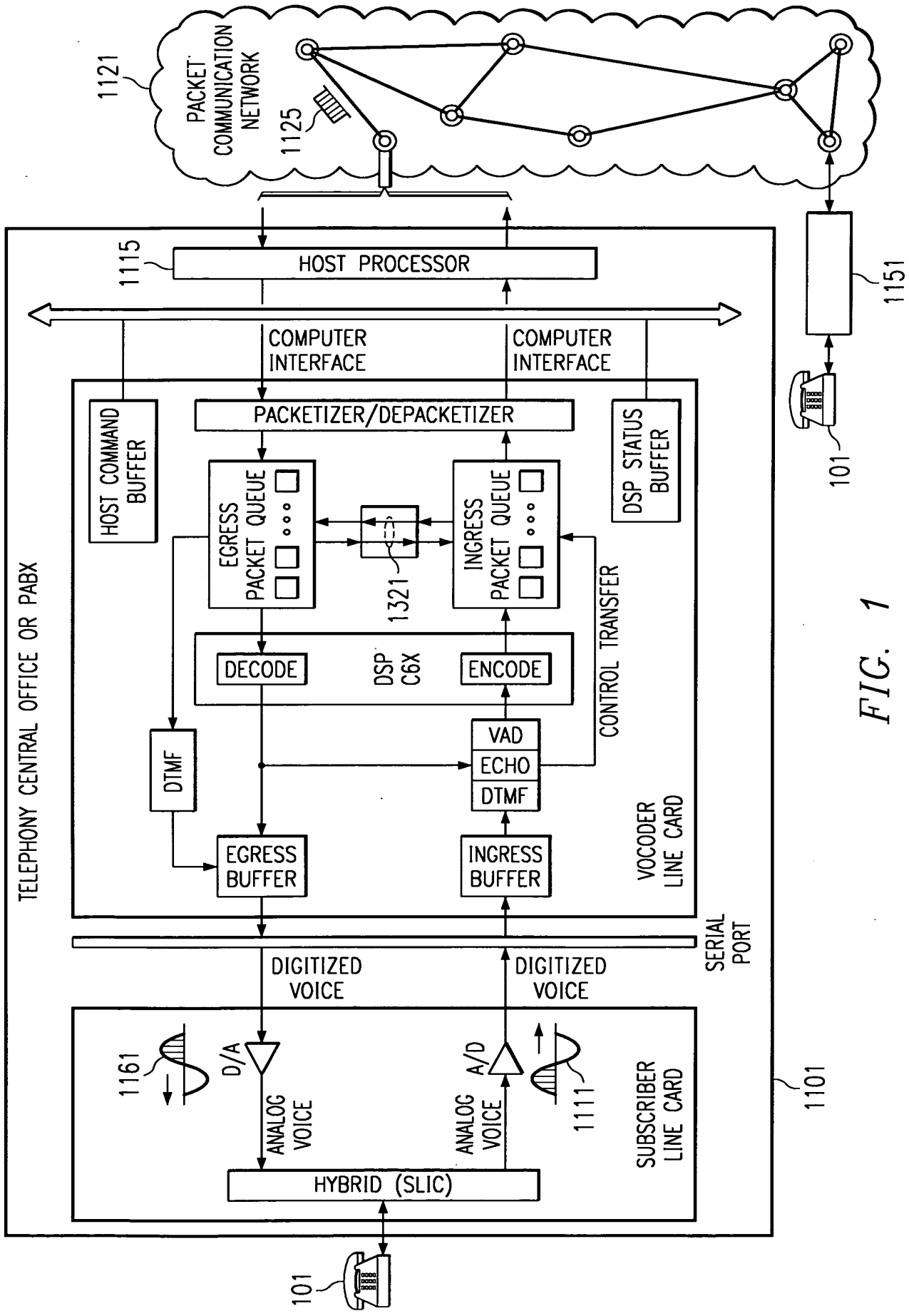

1121
PACKET COMMUNICATION NETWORK
1125
1115
HOST PROCESSOR
COMPUTER INTERFACE
COMPUTER INTERFACE
1151
101
HOST COMMAND BUFFER
PACKETIZER/DEPACKETIZER
DSP STATUS BUFFER
EGRESS PACKET QUEUE
INGRESS PACKET QUEUE
1321
CONTROL TRANSFER
DECODE
DSP C6X
ENCODE
VAD
ECHO
DTMF
DTMF
EGRESS BUFFER
INGRESS BUFFER
VOCODER LINE CARD
TELEPHONY CENTRAL OFFICE OR PABX
SERIAL PORT
DIGITIZED VOICE
DIGITIZED VOICE
1161
D/A
A/D
1111
ANALOG VOICE
ANALOG VOICE
SUBSCRIBER LINE CARD
1101
HYBRID (SLIC)
101

FIG. 1

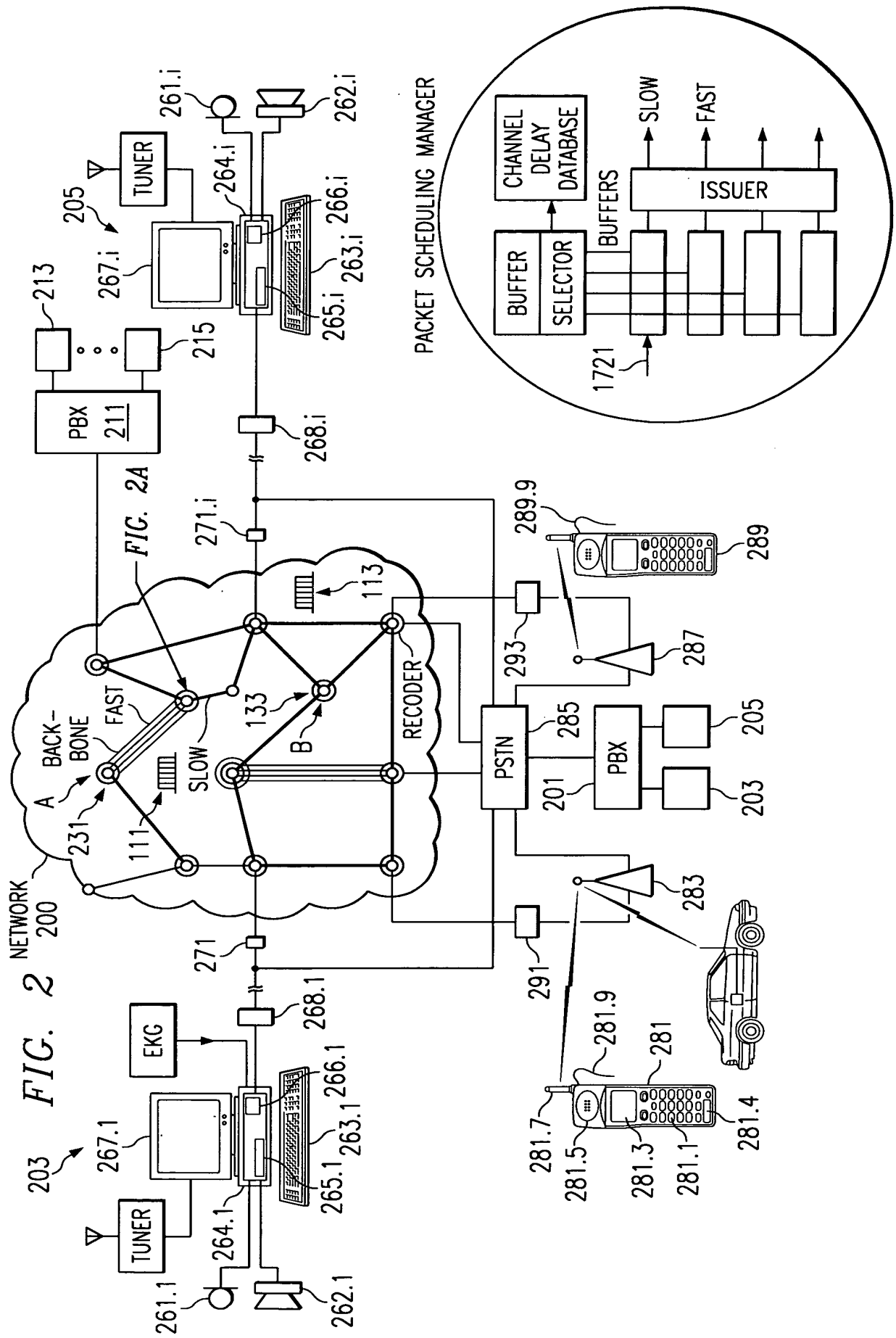

NETWORK 200
BACK-BONE
A
B
FAST
SLOW
231
111
133
113
RECODER
271
271.i
268.1
268.i
PBX 211
213
215
PSTN
285
201
PBX
205
203
289
289.9
287
293
283
291
281
281.1
281.3
281.4
281.5
281.7
281.9
203
205
TUNER
EKC
261.1
261.i
262.1
262.i
263.1
263.i
264.1
264.i
265.1
265.i
266.1
266.i
267.1
267.i
PACKET SCHEDULING MANAGER
CHANNEL DELAY DATABASE
BUFFER SELECTOR
BUFFERS
ISSUER
SLOW
FAST
1721

FIG. 2

FIG. 2A

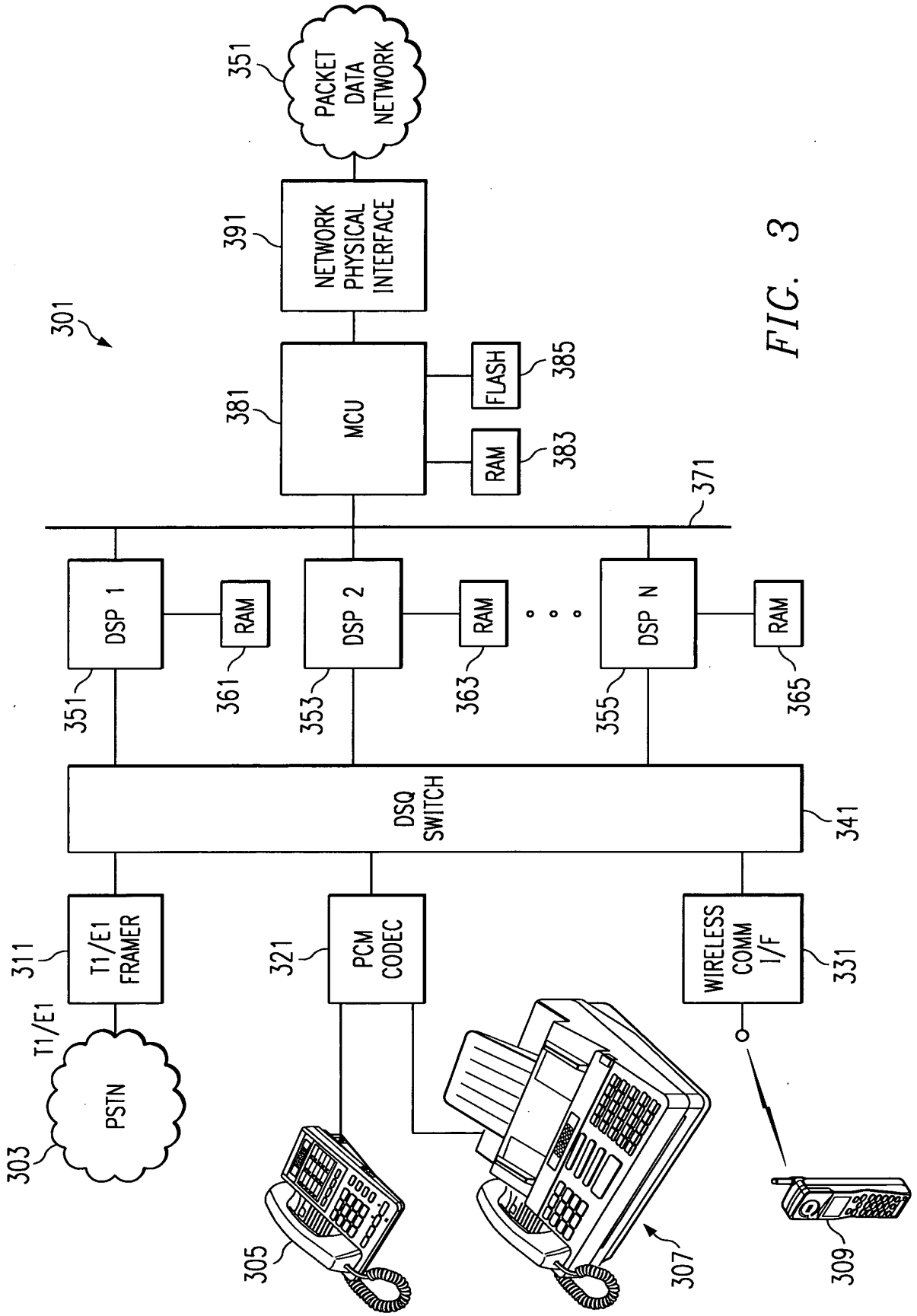

PACKET DATA NETWORK
351
NETWORK PHYSICAL INTERFACE
391
301
MCU
381
FLASH
385
RAM
383
371
DSP 1
RAM
361
351
DSP 2
RAM
363
353
DSP N
RAM
365
355
DSQ SWITCH
341
T1/E1 FRAMER
311
PCM CODEC
321
WIRELESS COMM I/F
331
T1/E1
PSTN
303
305
307
309

FIG. 3

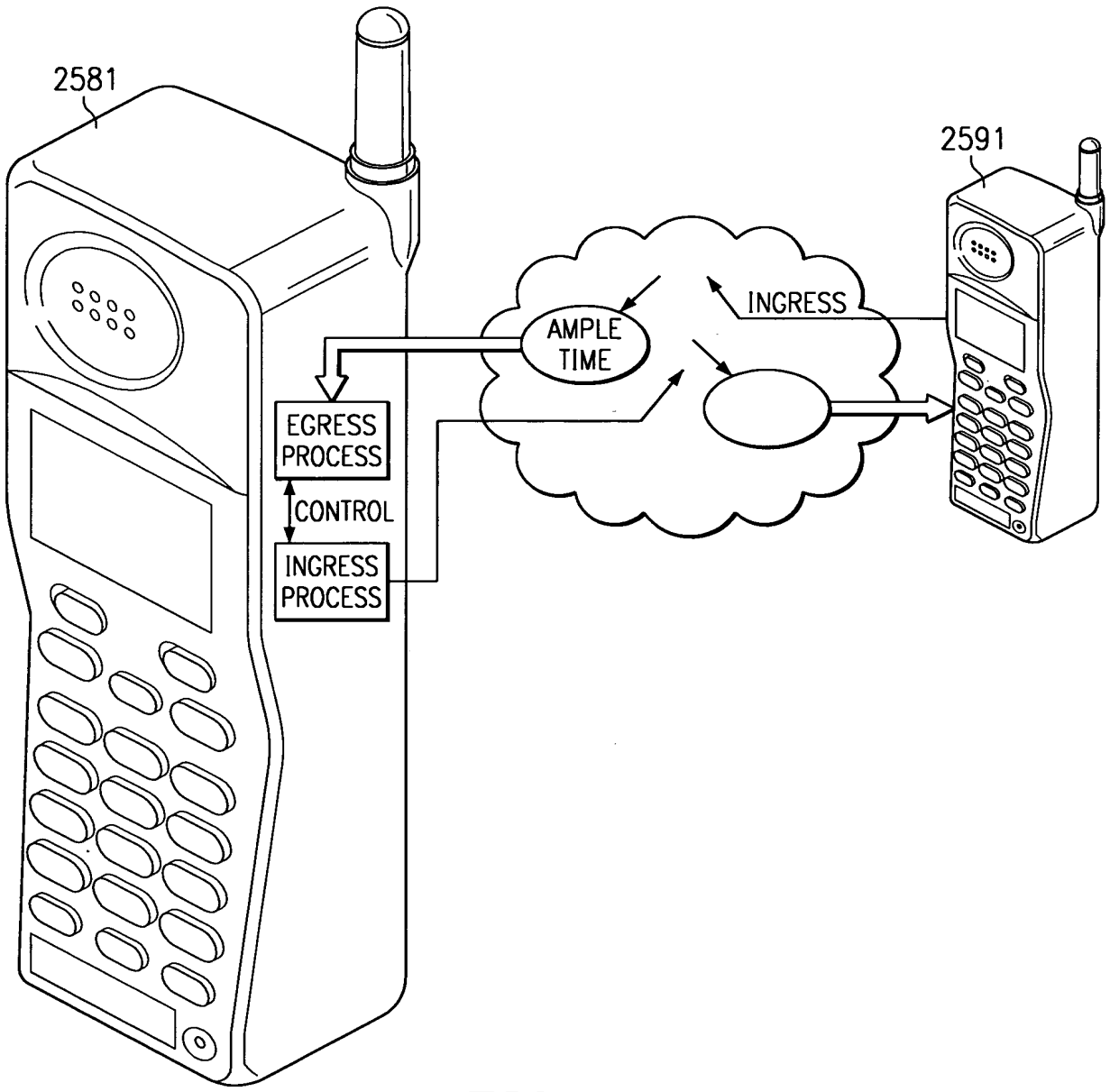

2581
2591
AMPLE TIME
INGRESS
EGRESS PROCESS
CONTROL
INGRESS PROCESS

FIG. 4

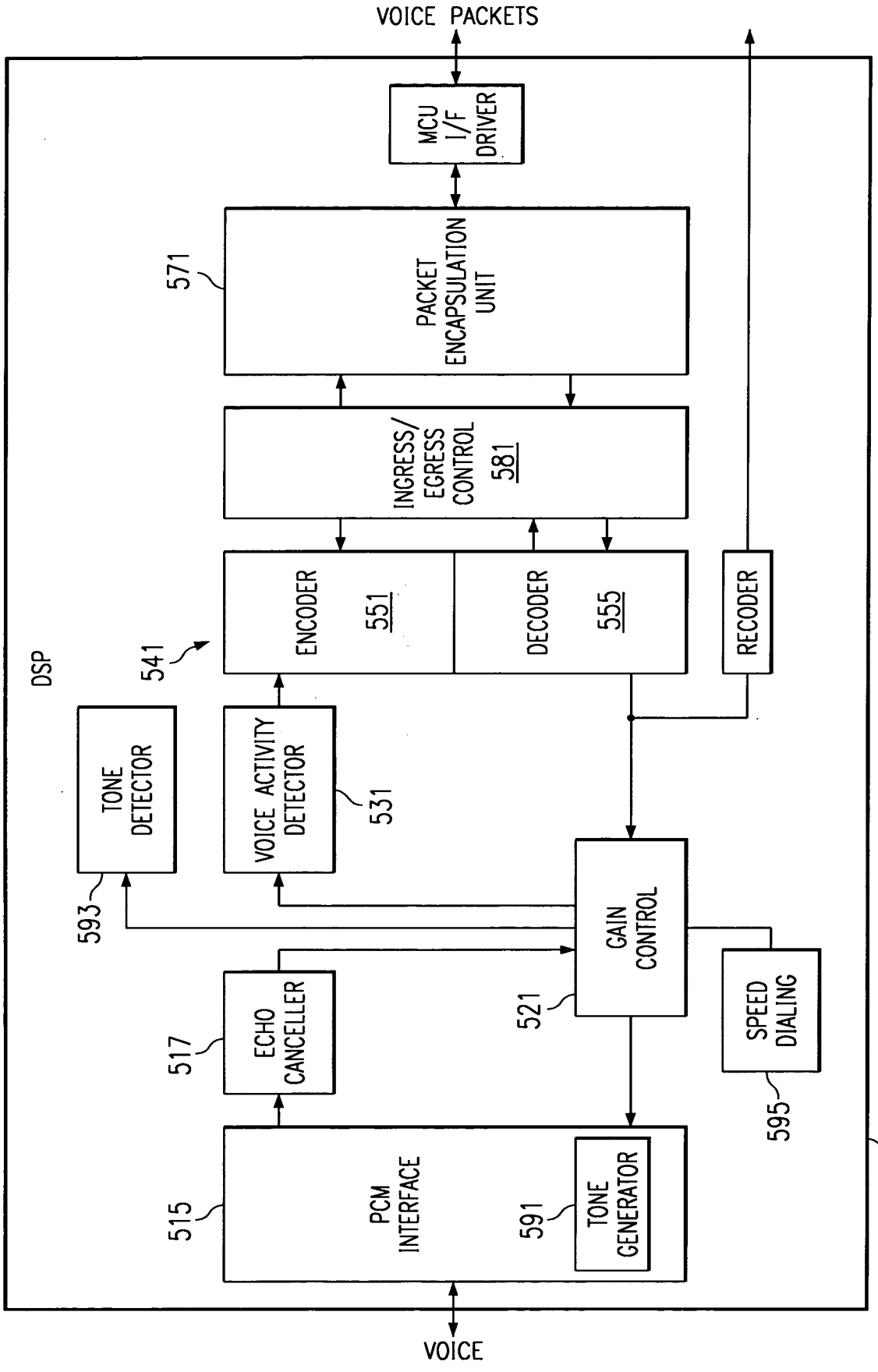

VOICE PACKETS
MCU I/F DRIVER
571
PACKET ENCAPSULATION UNIT
INGRESS/ EGRESS CONTROL 581
ENCODER 551
DECODER 555
RECODER
541
DSP
TONE DETECTOR
VOICE ACTIVITY DETECTOR
531
593
GAIN CONTROL
521
ECHO CANCELLER
517
SPEED DIALING
595
515
PCM INTERFACE
591
TONE GENERATOR
511
VOICE

FIG. 5

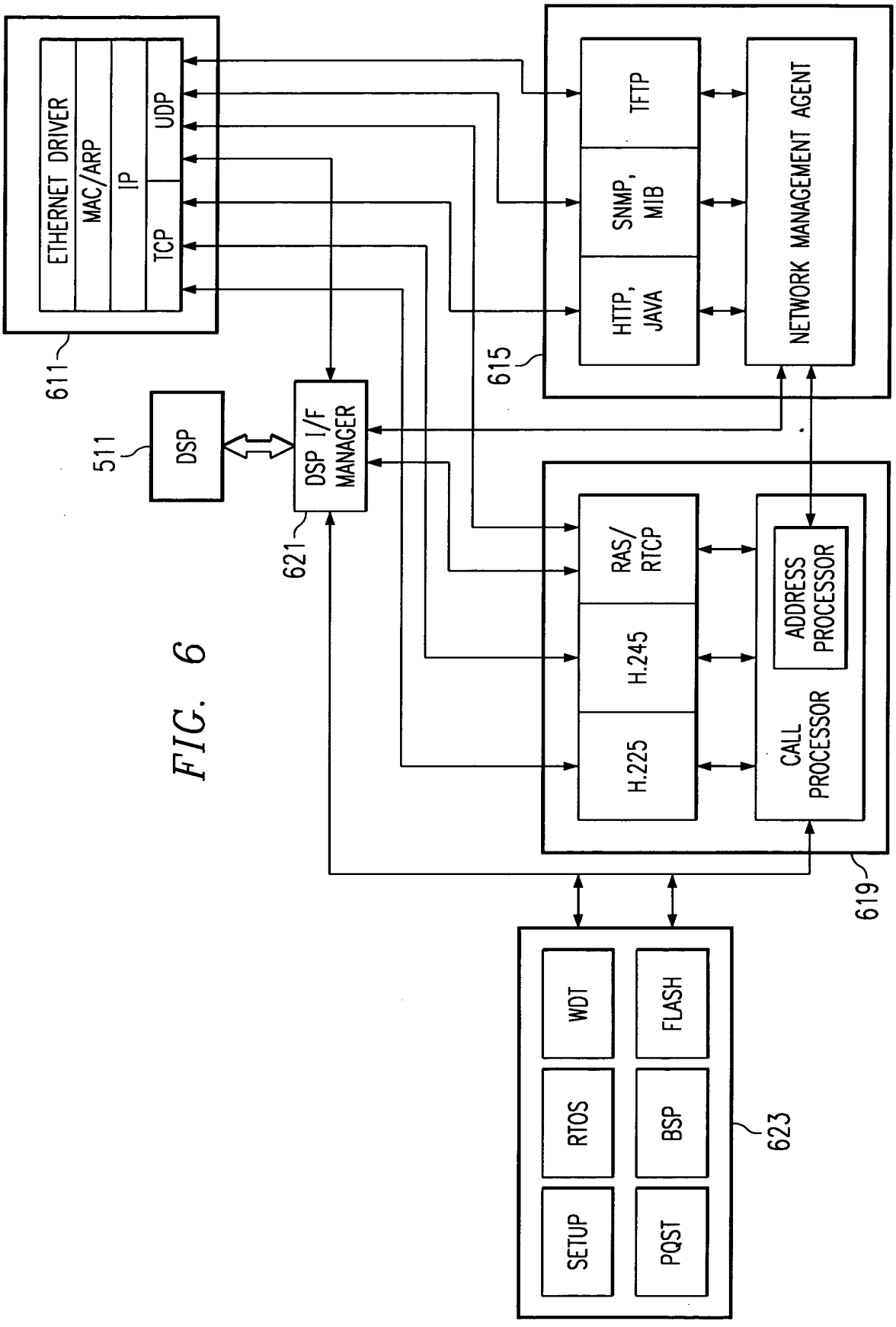

ETHERNET DRIVER
MAC/ARP
IP
TCP
UDP
611
DSP
511
DSP I/F MANAGER
621
TFTP
SNMP, MIB
HTTP, JAVA
NETWORK MANAGEMENT AGENT
615
RAS/ RTCP
H.245
H.225
ADDRESS PROCESSOR
CALL PROCESSOR
619
WDT
FLASH
RTOS
BSP
SETUP
PQST
623

FIG. 6

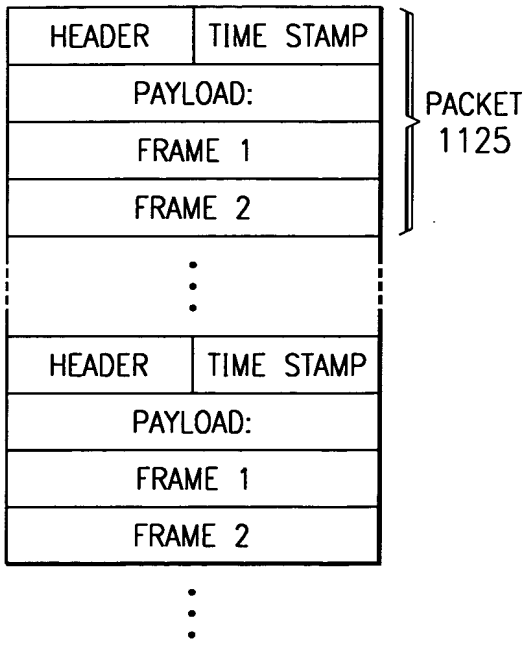

HEADER
TIME STAMP
PAYLOAD:
FRAME 1
FRAME 2
HEADER
TIME STAMP
PAYLOAD:
FRAME 1
FRAME 2
PACKET
1125

FIG. 7

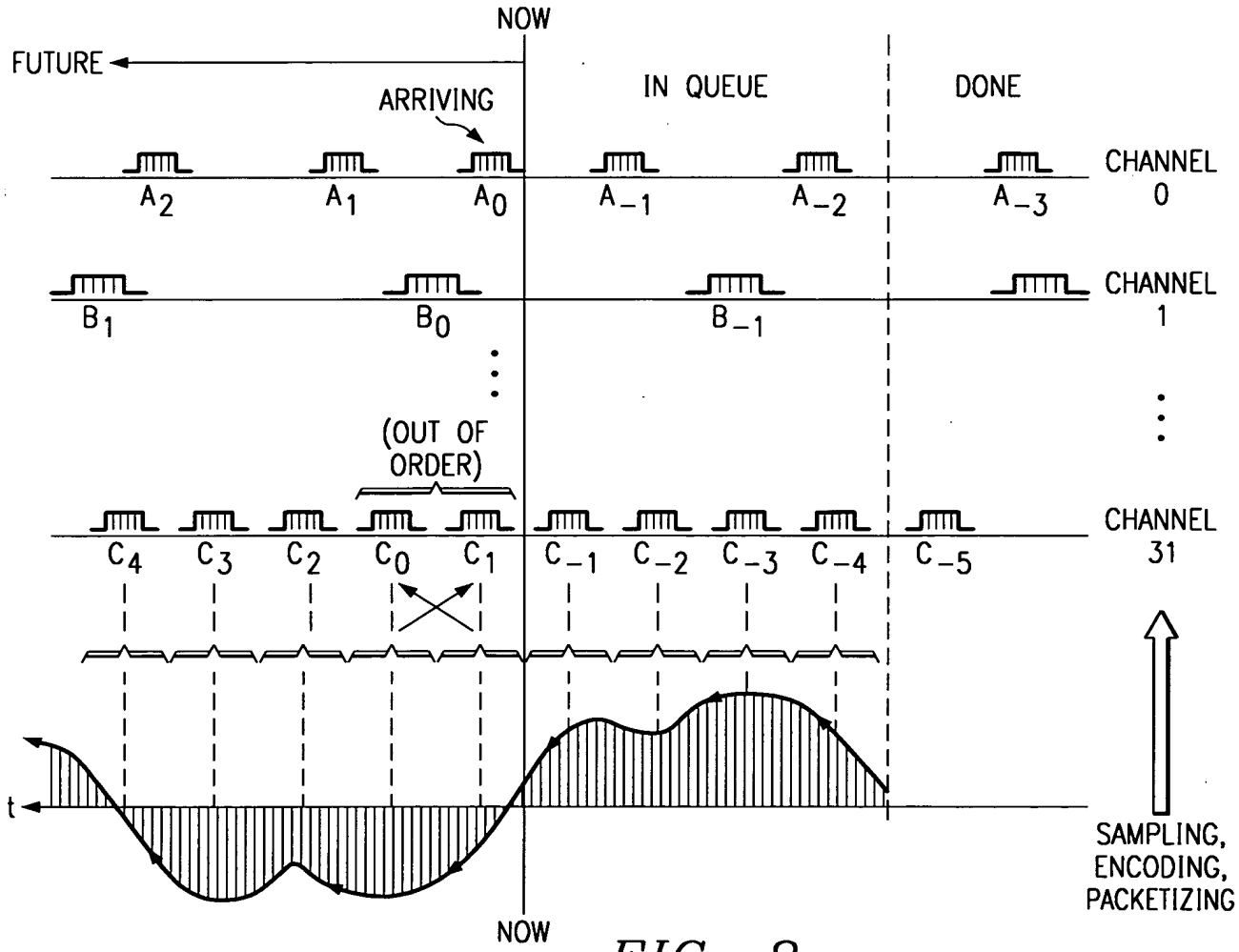

NOW
FUTURE
ARRIVING
IN QUEUE
DONE
CHANNEL 0
CHANNEL 1
CHANNEL 31
A2
A1
A0
A-1
A-2
A-3
B1
B0
B-1
(OUT OF ORDER)
C4
C3
C2
C0
C1
C-1
C-2
C-3
C-4
C-5
t
NOW
SAMPLING, ENCODING, PACKETIZING

FIG. 8

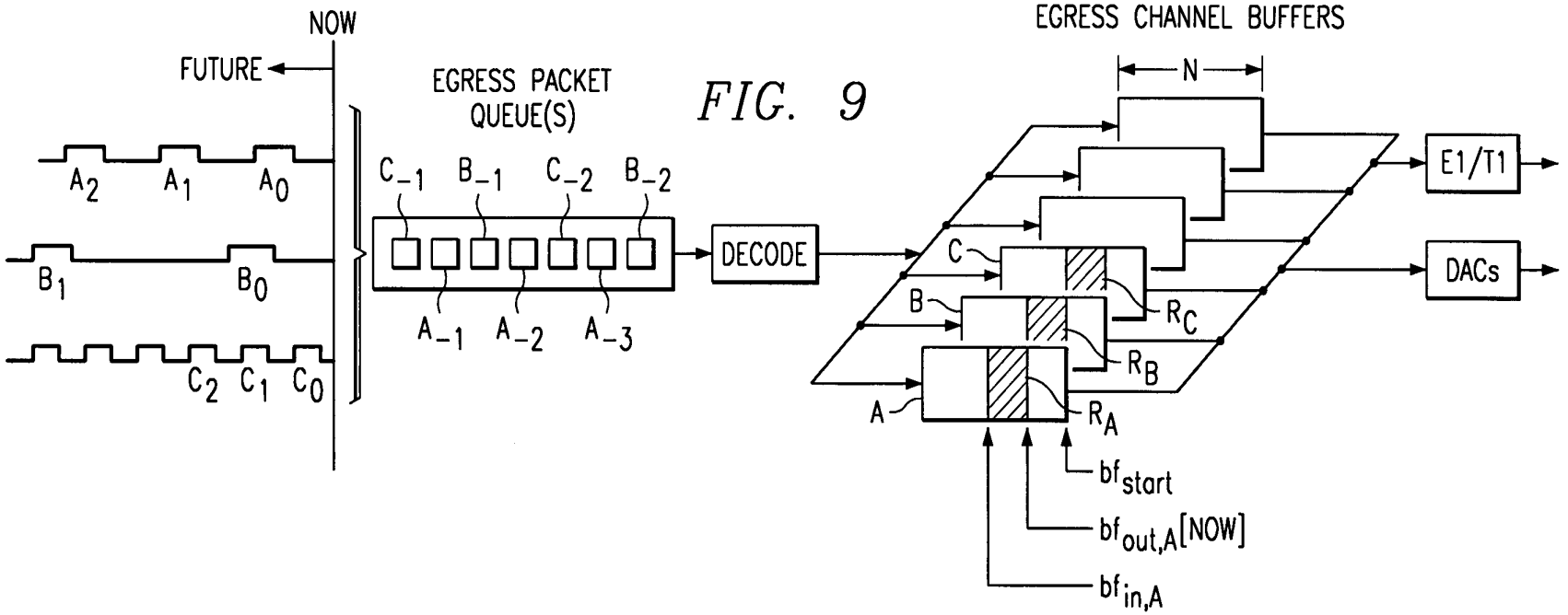

NOW
FUTURE
EGRESS PACKET QUEUE(S)
EGRESS CHANNEL BUFFERS
N
A_2 A_1 A_0
B_1 B_0
C_2 C_1 C_0
C_{-1} B_{-1} C_{-2} B_{-2}
A_{-1} A_{-2} A_{-3}
DECODE
C
B
A
R_C
R_B
R_A
E1/T1
DACs
bf_{start}
$bf_{out,A}[NOW]$
$bf_{in,A}$

FIG. 9

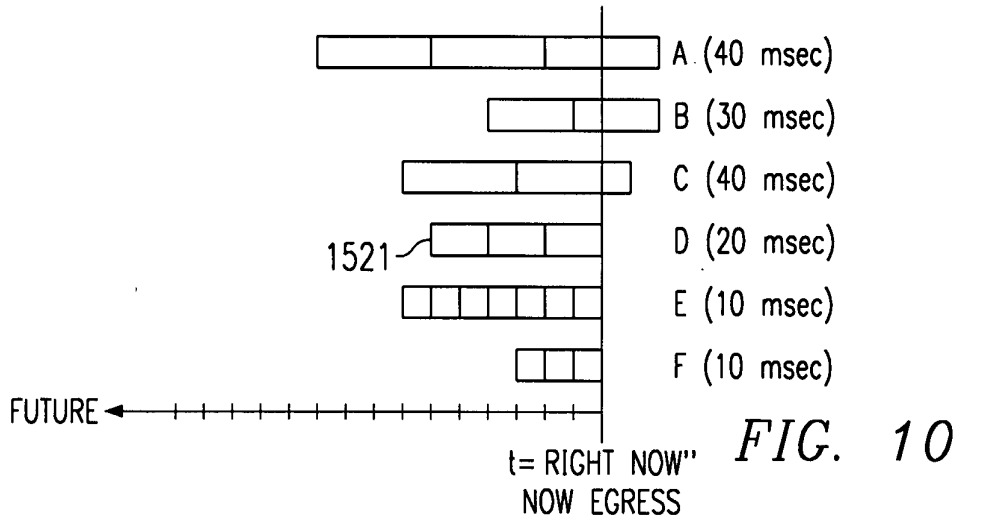

A (40 msec)
B (30 msec)
C (40 msec)
1521
D (20 msec)
E (10 msec)
F (10 msec)
FUTURE
t= RIGHT NOW"
NOW EGRESS

FIG. 10

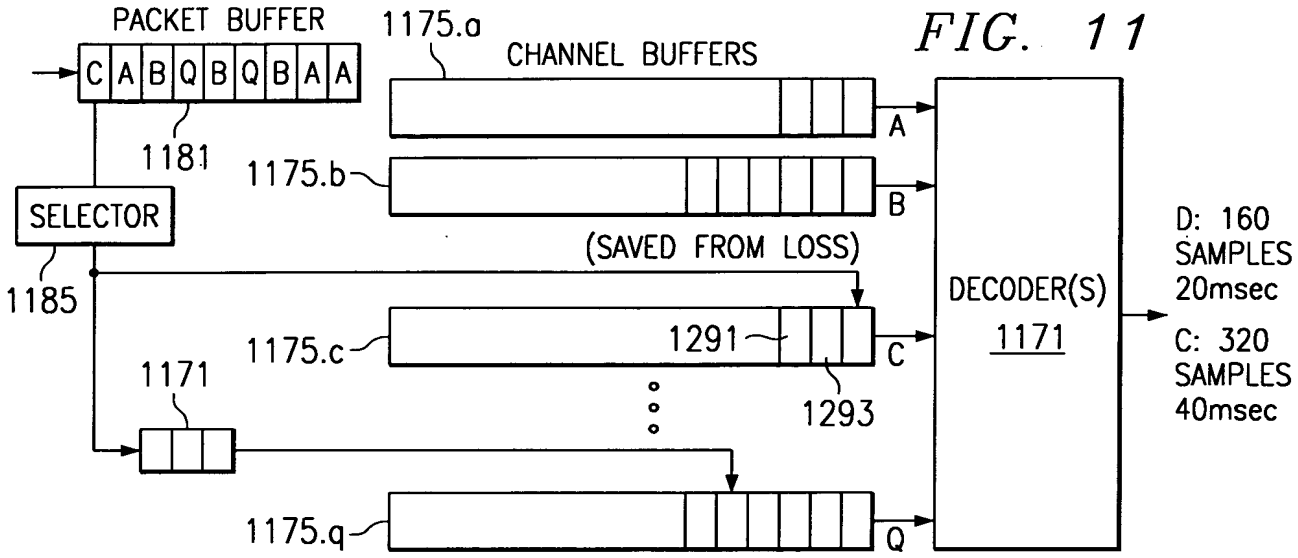


FIG. 11

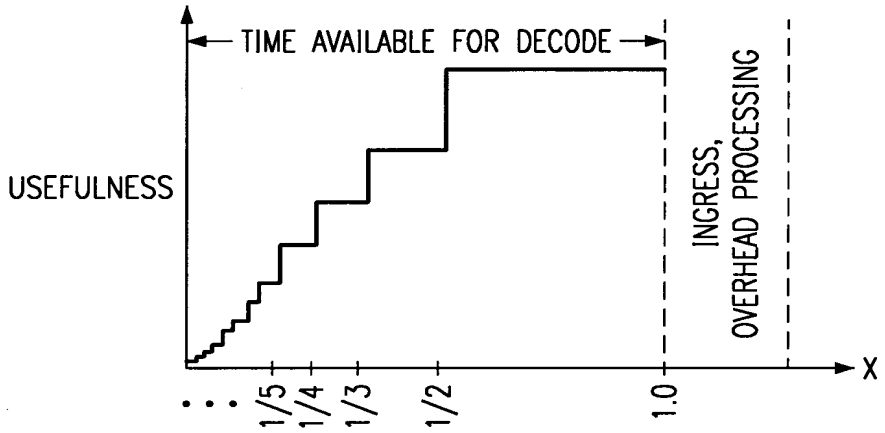


FIG. 12

$$X = \frac{\text{DECODE EXECUTE TIME}}{\text{TIME AVAILABLE FOR DECODE}}$$

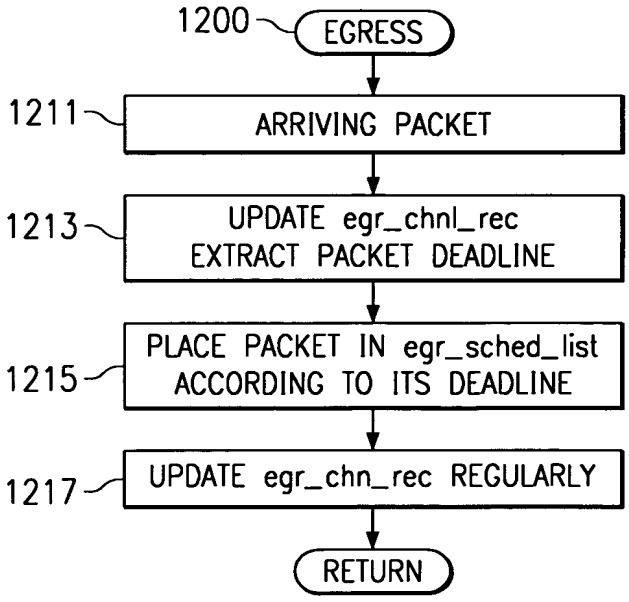


FIG. 13

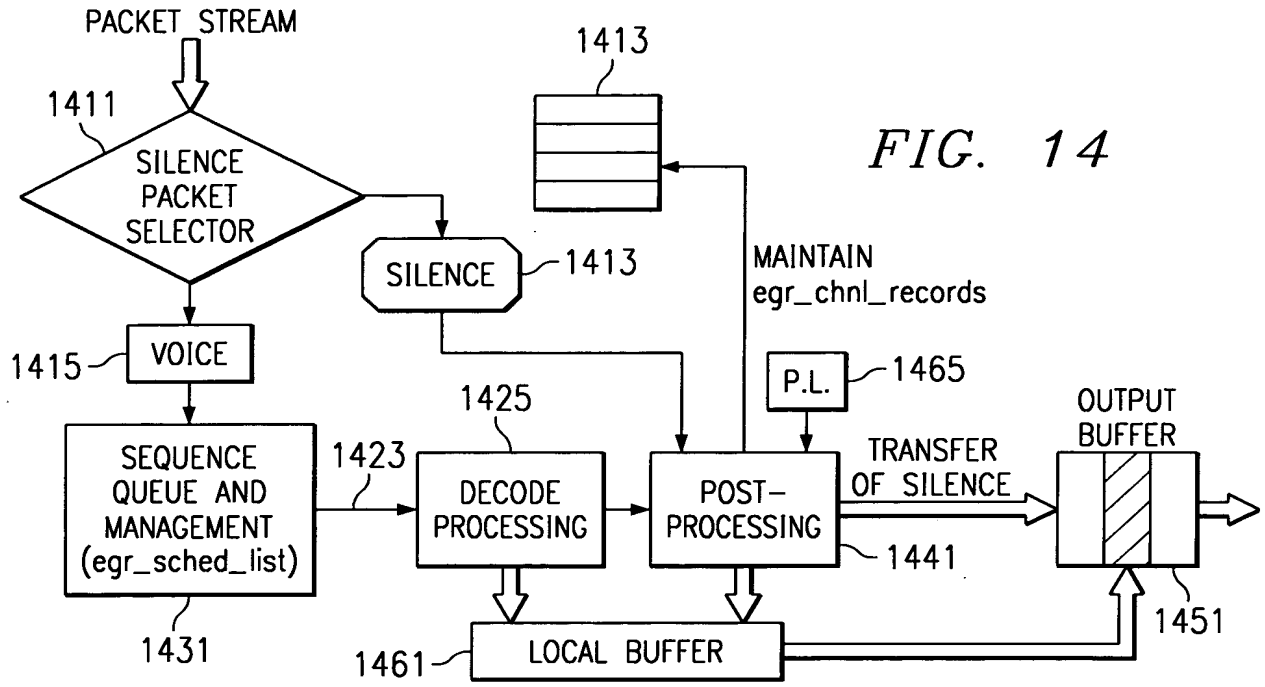

PACKET STREAM
1411
SILENCE PACKET SELECTOR
1413
SILENCE
1413
MAINTAIN egr_chnl_records
1415
VOICE
P.L.
1465
1425
OUTPUT BUFFER
SEQUENCE QUEUE AND MANAGEMENT (egr_sched_list)
1423
DECODE PROCESSING
POST-PROCESSING
TRANSFER OF SILENCE
1441
1431
1461
LOCAL BUFFER
1451

FIG. 14

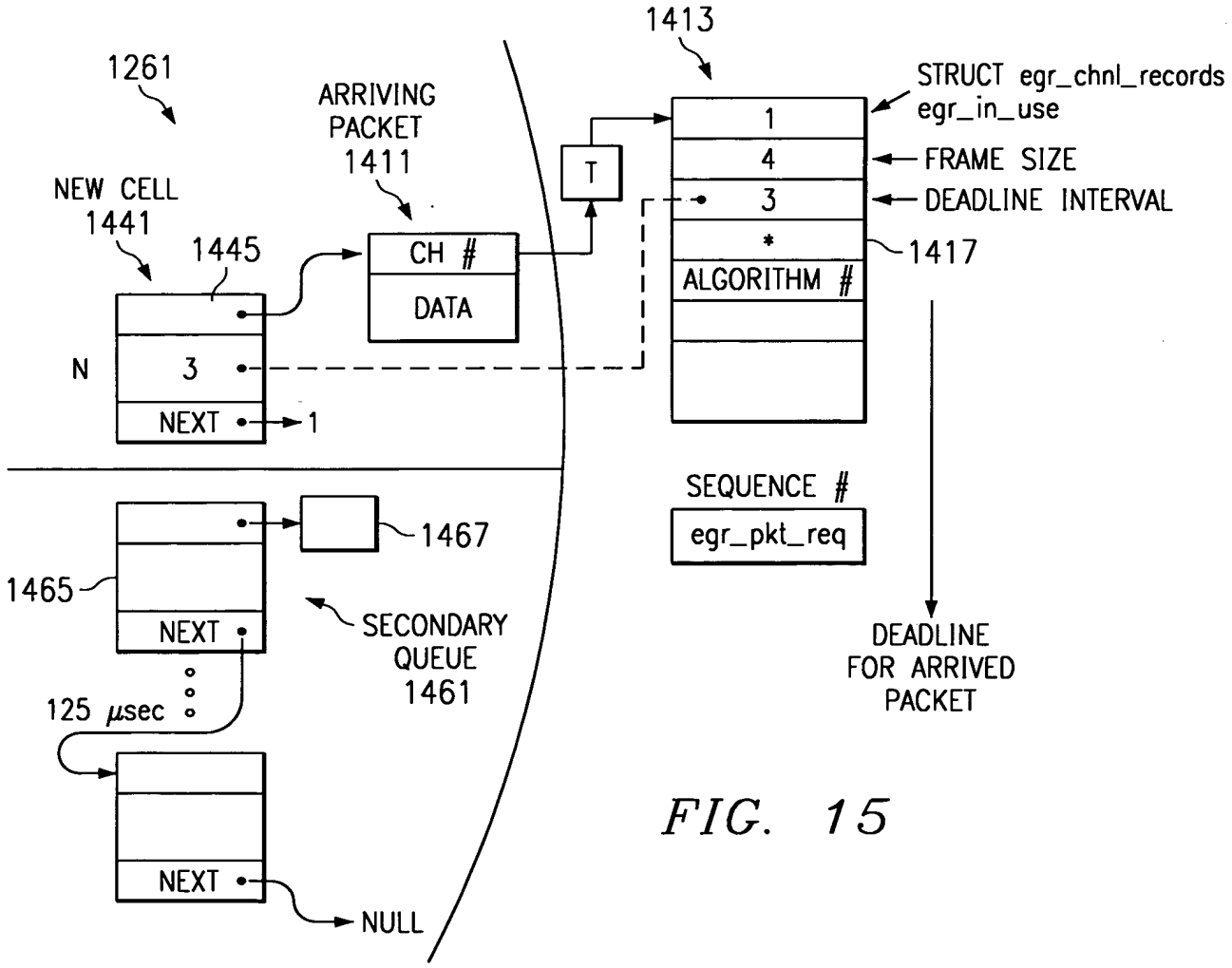

1413
1261
ARRIVING PACKET 1411
STRUCT egr_chnl_records
egr_in_use
1
4
FRAME SIZE
3
DEADLINE INTERVAL
*
1417
ALGORITHM #
NEW CELL 1441
1445
CH #
DATA
T
N
3
NEXT
1
SEQUENCE #
egr_pkt_req
1467
1465
NEXT
SECONDARY QUEUE 1461
125 μsec
DEADLINE FOR ARRIVED PACKET
NEXT
NULL

FIG. 15

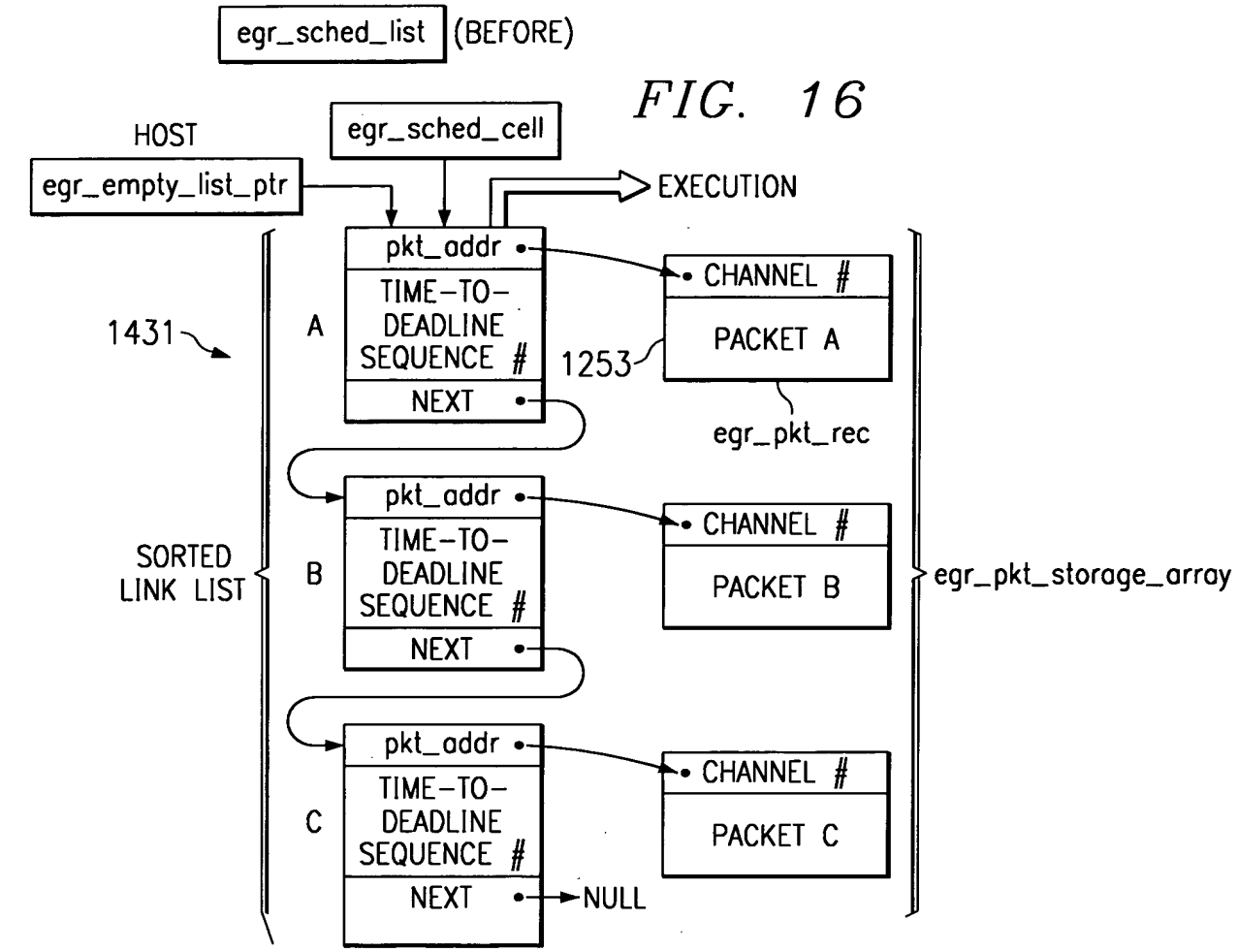


FIG. 16

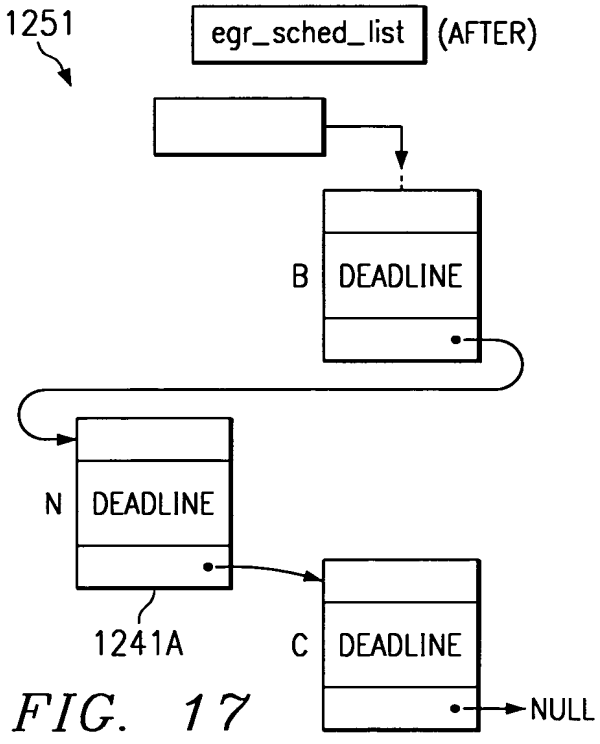


FIG. 17

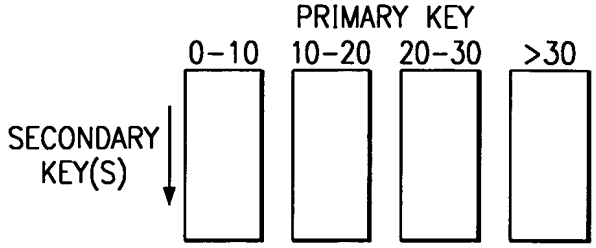


FIG. 18

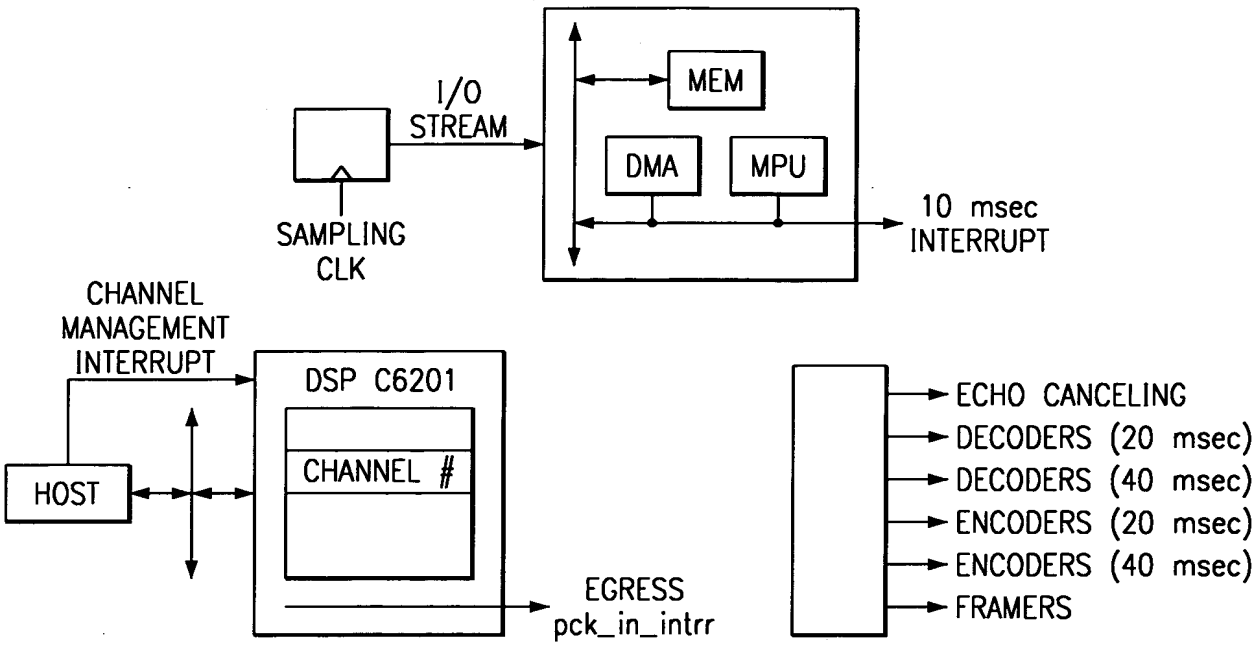

I/O
STREAM
SAMPLING
CLK
MEM
DMA
MPU
10 msec
INTERRUPT
CHANNEL
MANAGEMENT
INTERRUPT
DSP C6201
CHANNEL #
HOST
EGRESS
pck_in_intrr
ECHO CANCELING
DECODERS (20 msec)
DECODERS (40 msec)
ENCODERS (20 msec)
ENCODERS (40 msec)
FRAMERS

FIG. 19

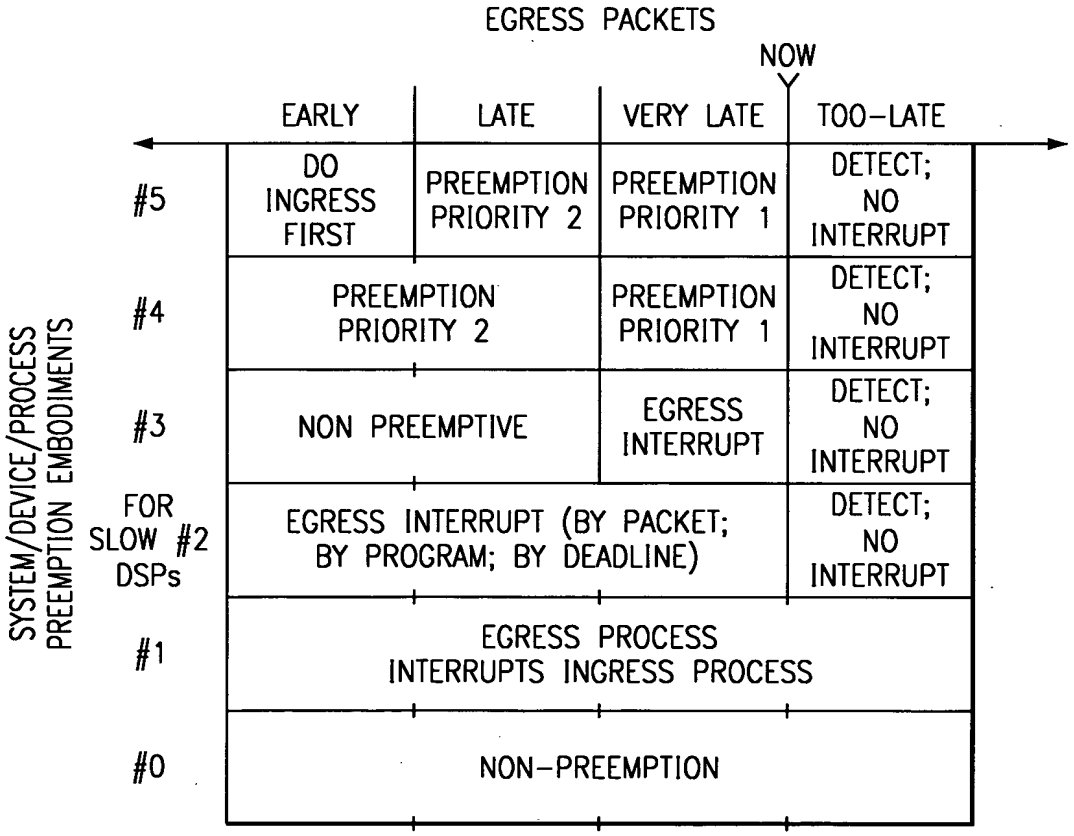

EGRESS PACKETS
NOW
EARLY
LATE
VERY LATE
TOO-LATE
SYSTEM/DEVICE/PROCESS
PREEMPTION EMBODIMENTS
#5
DO
INGRESS
FIRST
PREEMPTION
PRIORITY 2
PREEMPTION
PRIORITY 1
DETECT;
NO
INTERRUPT
#4
PREEMPTION
PRIORITY 2
PREEMPTION
PRIORITY 1
DETECT;
NO
INTERRUPT
#3
NON PREEMPTIVE
EGRESS
INTERRUPT
DETECT;
NO
INTERRUPT
FOR
SLOW #2
DSPs
EGRESS INTERRUPT (BY PACKET;
BY PROGRAM; BY DEADLINE)
DETECT;
NO
INTERRUPT
#1
EGRESS PROCESS
INTERRUPTS INGRESS PROCESS
#0
NON-PREEMPTION

FIG. 20

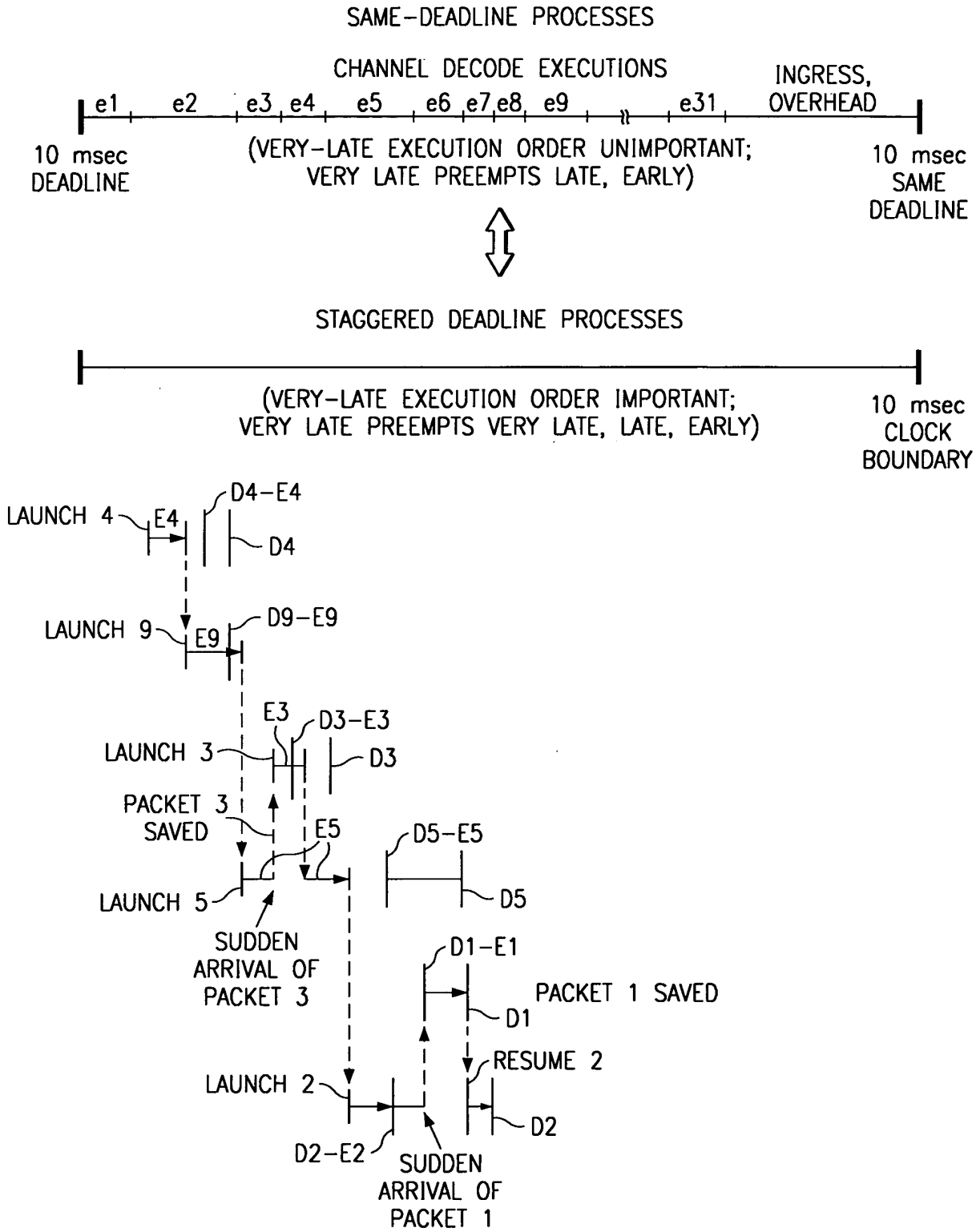

SAME-DEADLINE PROCESSES
CHANNEL DECODE EXECUTIONS
INGRESS, OVERHEAD
e1
e2
e3
e4
e5
e6
e7
e8
e9
e31
10 msec DEADLINE
(VERY-LATE EXECUTION ORDER UNIMPORTANT; VERY LATE PREEMPTS LATE, EARLY)
10 msec SAME DEADLINE
STAGGERED DEADLINE PROCESSES
(VERY-LATE EXECUTION ORDER IMPORTANT; VERY LATE PREEMPTS VERY LATE, LATE, EARLY)
10 msec CLOCK BOUNDARY
LAUNCH 4
E4
D4-E4
D4
LAUNCH 9
E9
D9-E9
E3
D3-E3
LAUNCH 3
D3
PACKET 3 SAVED
E5
D5-E5
LAUNCH 5
D5
SUDDEN ARRIVAL OF PACKET 3
D1-E1
PACKET 1 SAVED
D1
RESUME 2
LAUNCH 2
D2
D2-E2
SUDDEN ARRIVAL OF PACKET 1

FIG. 21

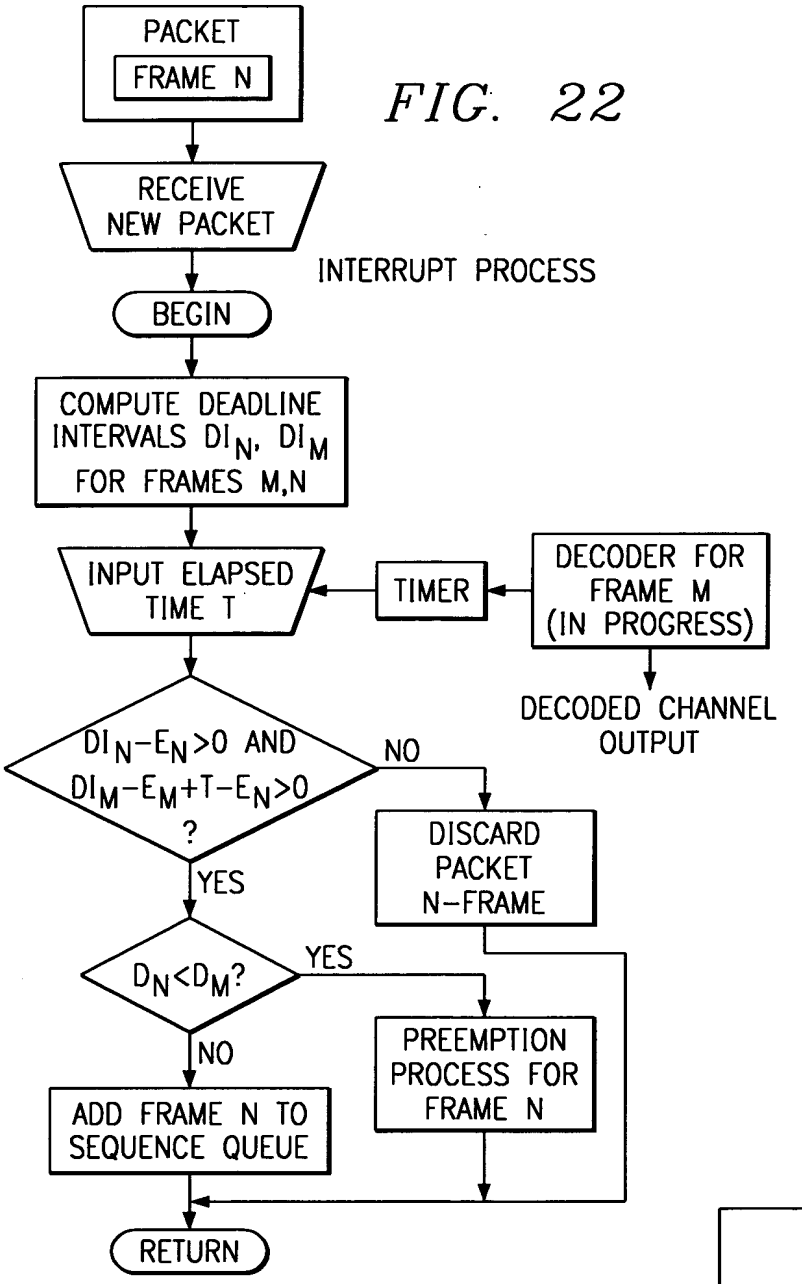

PACKET
FRAME N
RECEIVE NEW PACKET
INTERRUPT PROCESS
BEGIN
COMPUTE DEADLINE INTERVALS DI_N, DI_M FOR FRAMES M,N
INPUT ELAPSED TIME T
TIMER
DECODER FOR FRAME M (IN PROGRESS)
DECODED CHANNEL OUTPUT
$DI_N-E_N>0$ AND $DI_M-E_M+T-E_N>0$?
NO
YES
DISCARD PACKET N-FRAME
$D_N<D_M$?
YES
NO
PREEMPTION PROCESS FOR FRAME N
ADD FRAME N TO SEQUENCE QUEUE
RETURN

FIG. 22

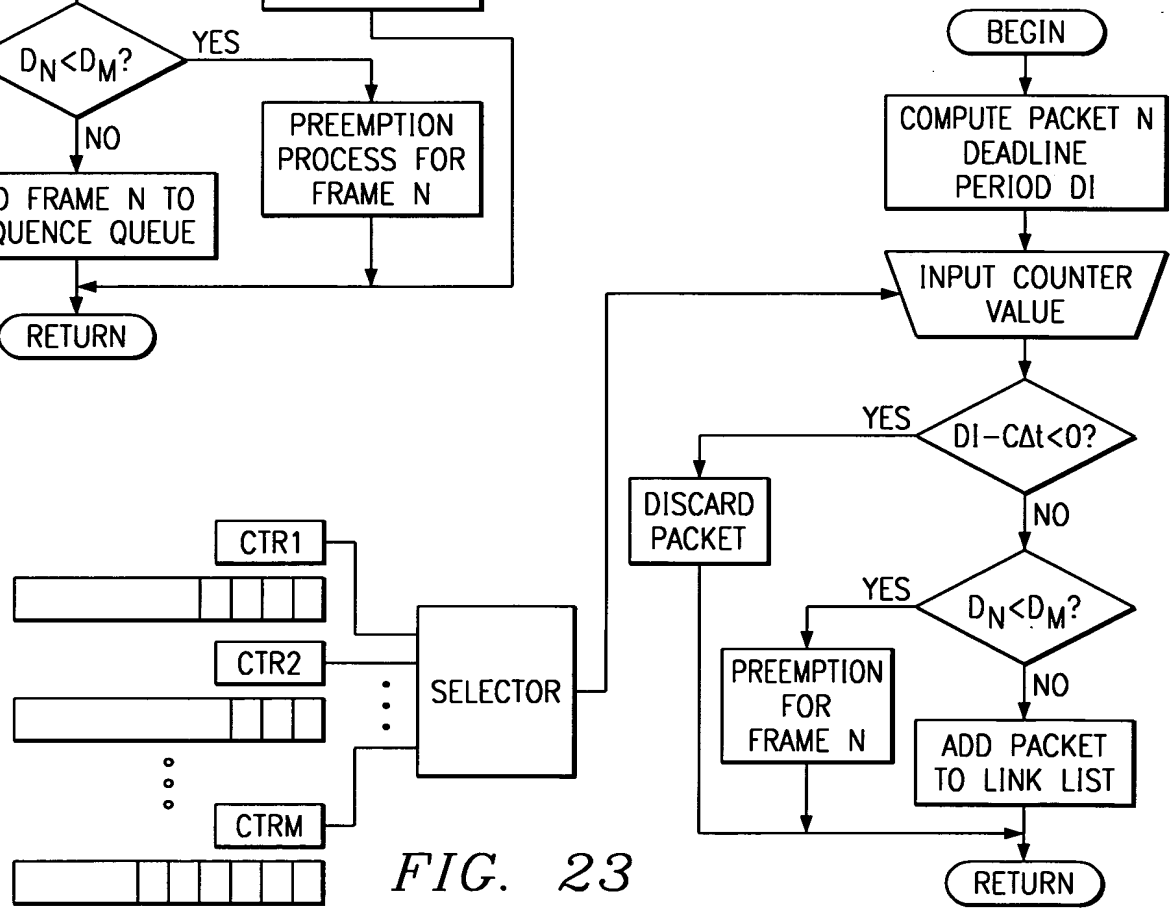

CTR1
CTR2
CTRM
SELECTOR
BEGIN
COMPUTE PACKET N DEADLINE PERIOD DI
INPUT COUNTER VALUE
YES
$DI-C\Delta t<0$?
NO
DISCARD PACKET
YES
$D_N<D_M$?
NO
PREEMPTION FOR FRAME N
ADD PACKET TO LINK LIST
RETURN

FIG. 23

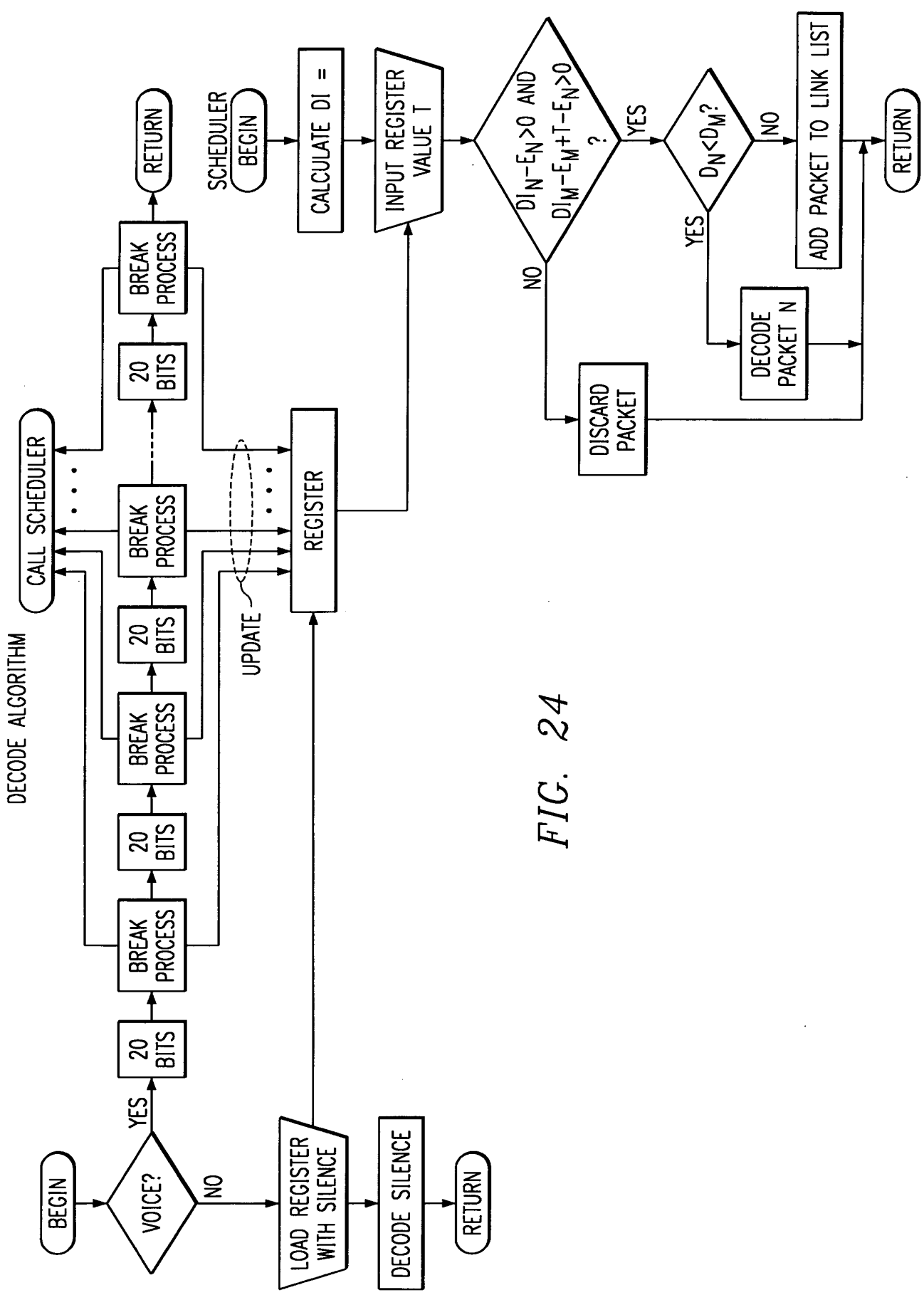

BEGIN
VOICE?
YES
NO
20 BITS
BREAK PROCESS
20 BITS
BREAK PROCESS
20 BITS
BREAK PROCESS
20 BITS
BREAK PROCESS
RETURN
CALL SCHEDULER
DECODE ALGORITHM
UPDATE
REGISTER
LOAD REGISTER WITH SILENCE
DECODE SILENCE
RETURN
SCHEDULER BEGIN
CALCULATE DI =
INPUT REGISTER VALUE T
DI_N-E_N>0 AND DI_M-E_M+T-E_N>0 ?
YES
NO
DISCARD PACKET
D_N<D_M?
YES
NO
DECODE PACKET N
ADD PACKET TO LINK LIST
RETURN

FIG. 24

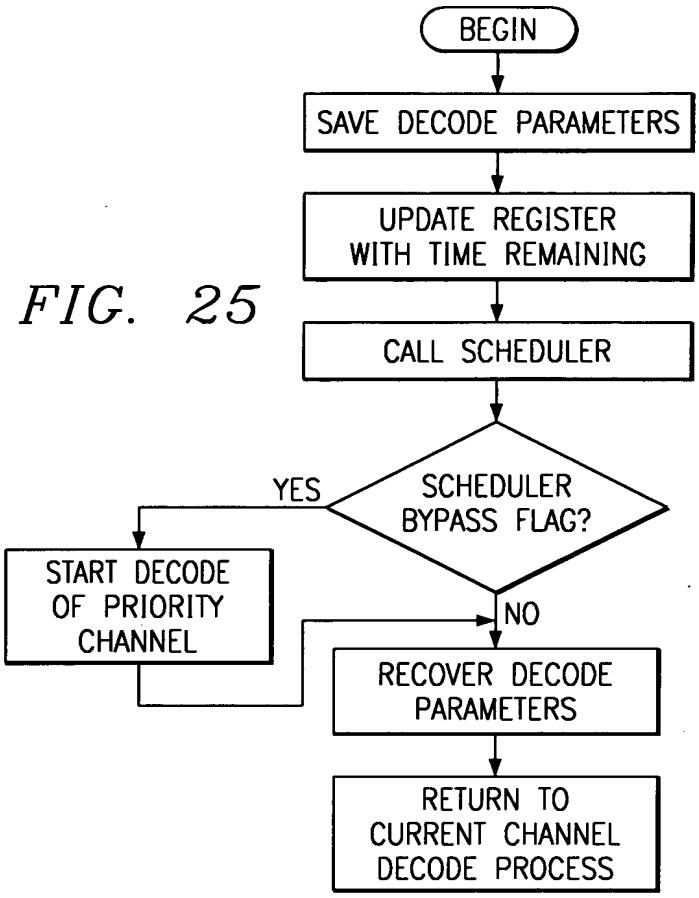

BEGIN
SAVE DECODE PARAMETERS
UPDATE REGISTER WITH TIME REMAINING
CALL SCHEDULER
SCHEDULER BYPASS FLAG?
YES
NO
START DECODE OF PRIORITY CHANNEL
RECOVER DECODE PARAMETERS
RETURN TO CURRENT CHANNEL DECODE PROCESS

FIG. 25

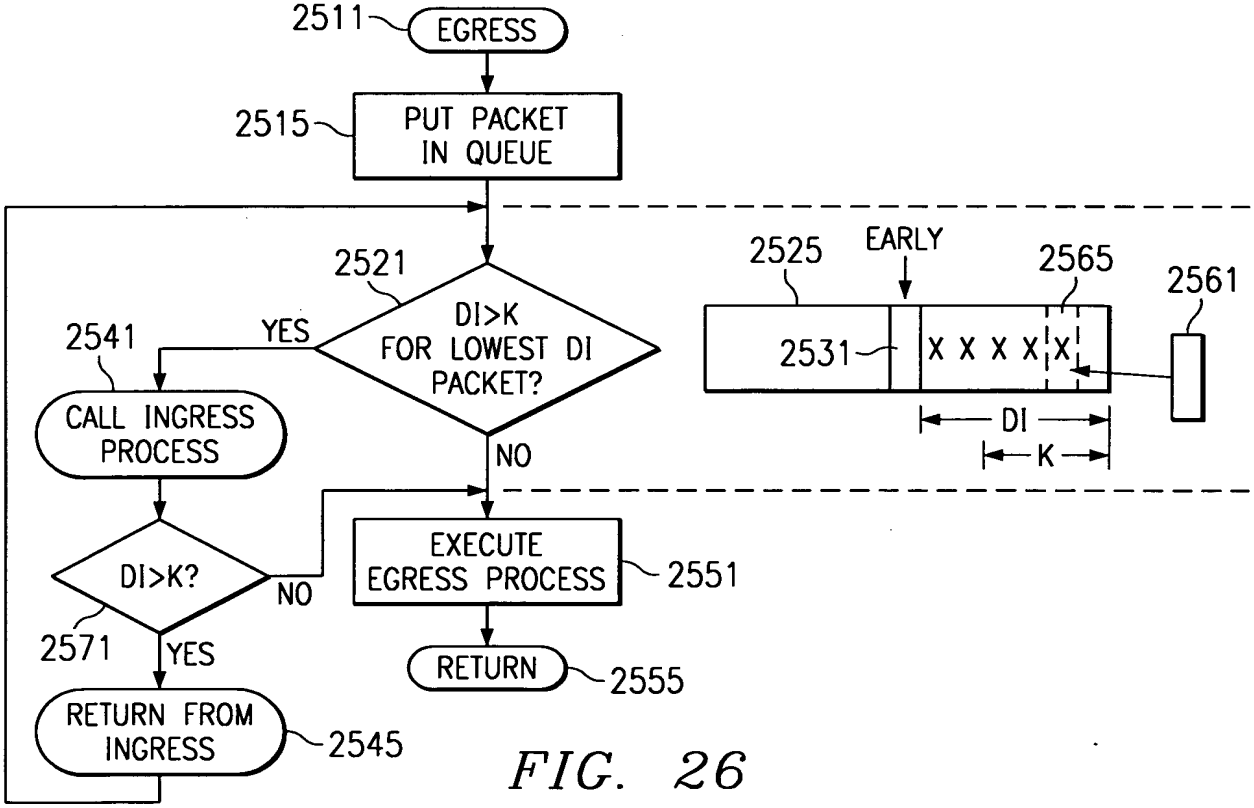

2511
EGRESS
2515
PUT PACKET IN QUEUE
2521
DI>K FOR LOWEST DI PACKET?
YES
NO
2541
CALL INGRESS PROCESS
DI>K?
NO
YES
2571
RETURN FROM INGRESS
2545
EXECUTE EGRESS PROCESS
2551
RETURN
2555
2525
EARLY
2565
2561
2531
X X X X X
DI
K

FIG. 26

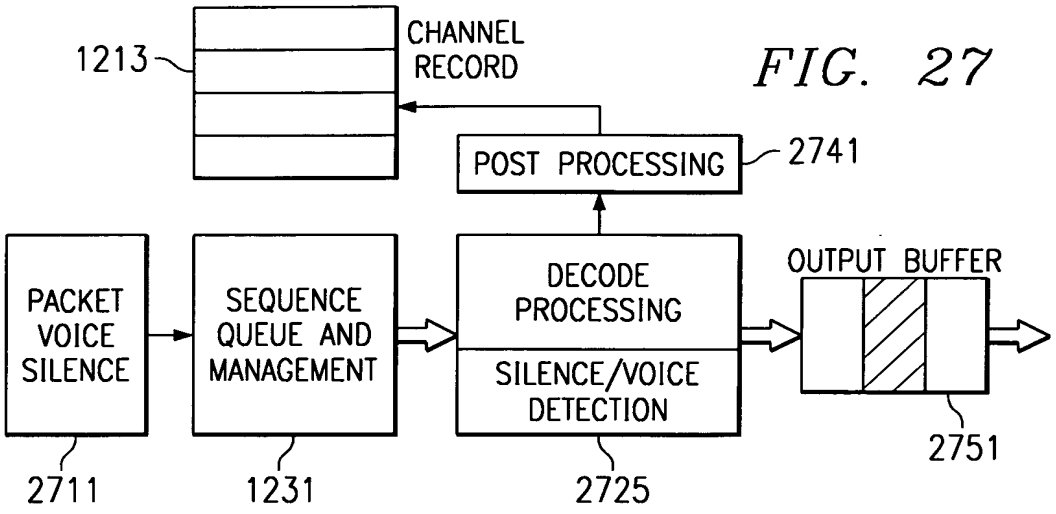

1213
CHANNEL RECORD
POST PROCESSING
2741
PACKET VOICE SILENCE
SEQUENCE QUEUE AND MANAGEMENT
DECODE PROCESSING
SILENCE/VOICE DETECTION
OUTPUT BUFFER
2751
2711
1231
2725

FIG. 27

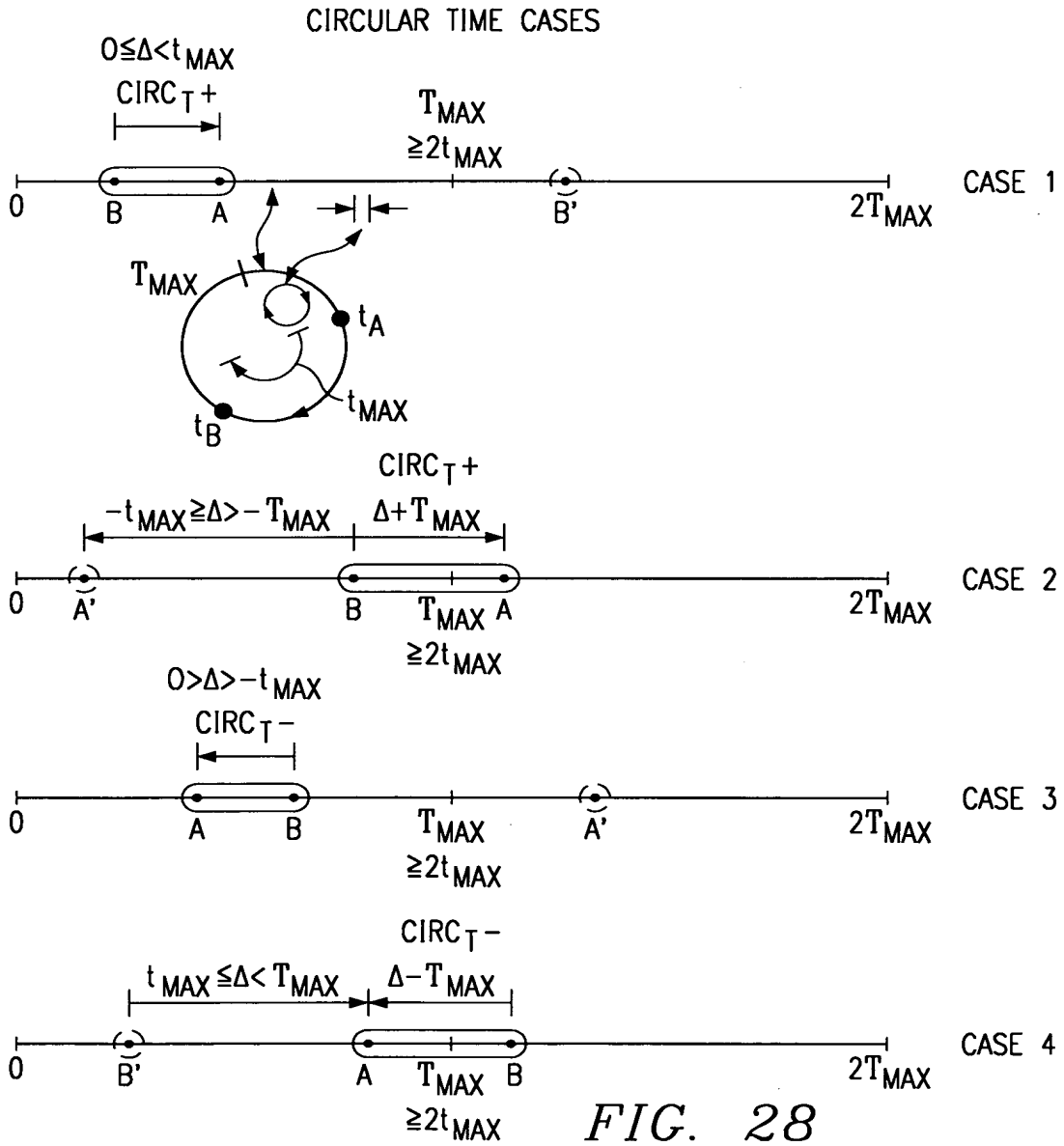

CIRCULAR TIME CASES
0≤Δ<t MAX
CIRC T +
T MAX
≥2t MAX
0
B
A
B'
2T MAX
CASE 1
T MAX
t A
t MAX
t B
CIRC T +
-t MAX≥Δ>-T MAX
Δ+T MAX
0
A'
B
T MAX
A
2T MAX
≥2t MAX
CASE 2
0>Δ>-t MAX
CIRC T -
0
A
B
T MAX
A'
2T MAX
≥2t MAX
CASE 3
CIRC T -
t MAX≤Δ< T MAX
Δ-T MAX
0
B'
A
T MAX
B
2T MAX
≥2t MAX
CASE 4

FIG. 28

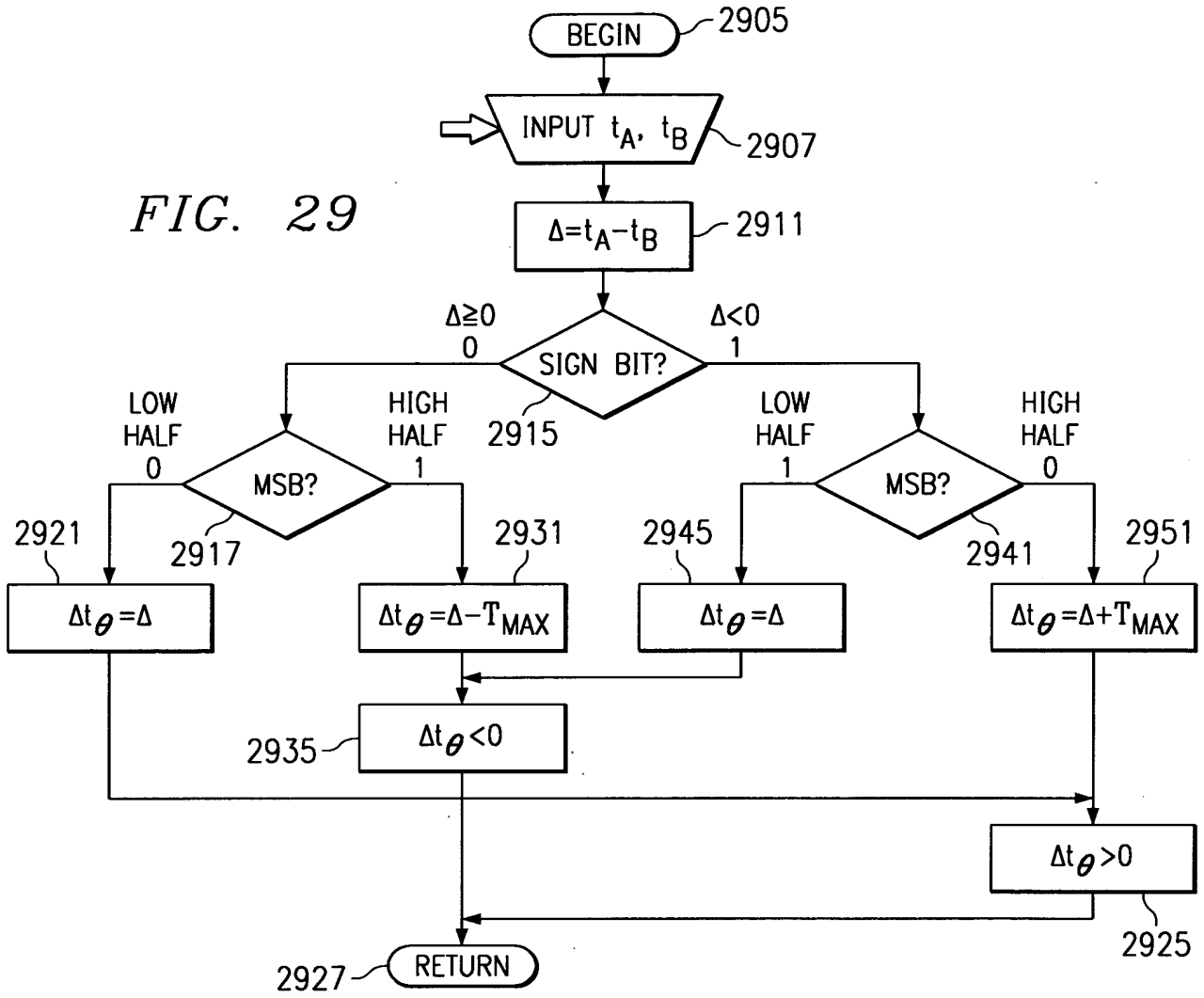

BEGIN
2905
INPUT t_A, t_B
2907
$\Delta=t_A-t_B$
2911
$\Delta\geq 0$
0
SIGN BIT?
$\Delta<0$
1
2915
LOW HALF
0
MSB?
HIGH HALF
1
2917
2921
2931
LOW HALF
1
MSB?
HIGH HALF
0
2941
2945
2951
$\Delta t_\theta=\Delta$
$\Delta t_\theta=\Delta-T_{MAX}$
$\Delta t_\theta=\Delta$
$\Delta t_\theta=\Delta+T_{MAX}$
2935
$\Delta t_\theta<0$
$\Delta t_\theta>0$
2925
2927
RETURN

FIG. 29

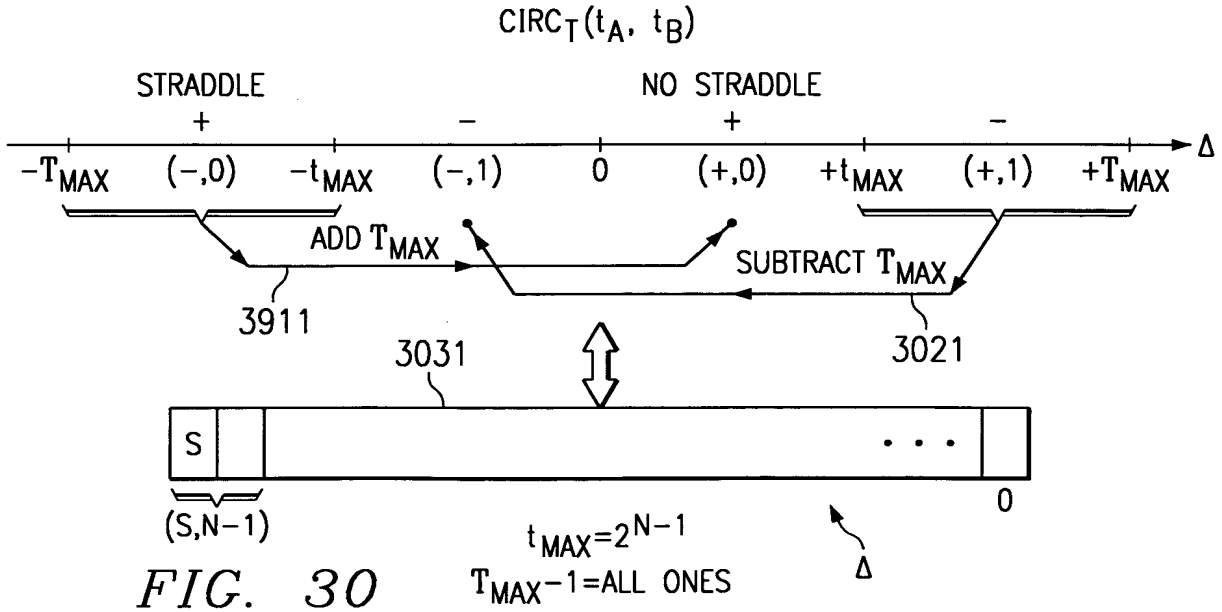

$CIRC_T(t_A, t_B)$
STRADDLE
NO STRADDLE
+
−
+
−
Δ
$-T_{MAX}$
(−,0)
$-t_{MAX}$
(−,1)
0
(+,0)
$+t_{MAX}$
(+,1)
$+T_{MAX}$
ADD T_{MAX}
SUBTRACT T_{MAX}
3911
3021
3031
S
0
(S,N−1)
$t_{MAX}=2^{N-1}$
$T_{MAX}-1$=ALL ONES
Δ

FIG. 30

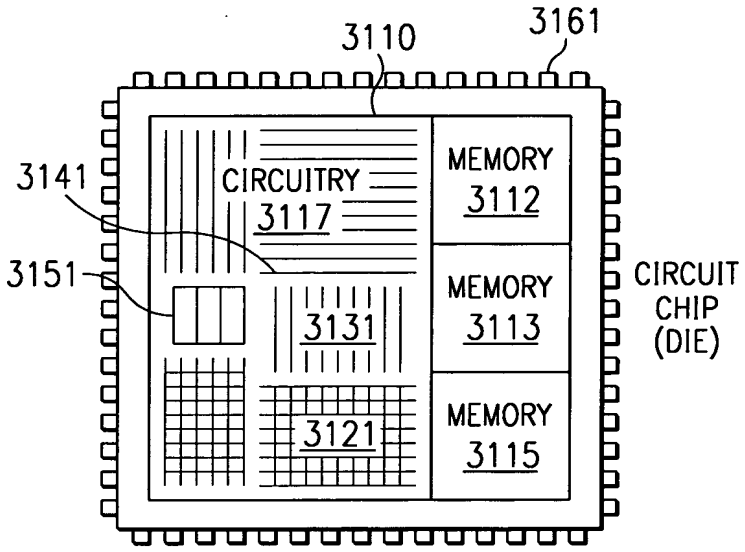

3110
3161
3141
3151
CIRCUITRY
3117
3131
3121
MEMORY
3112
MEMORY
3113
MEMORY
3115
CIRCUIT
CHIP
(DIE)

FIG. 31

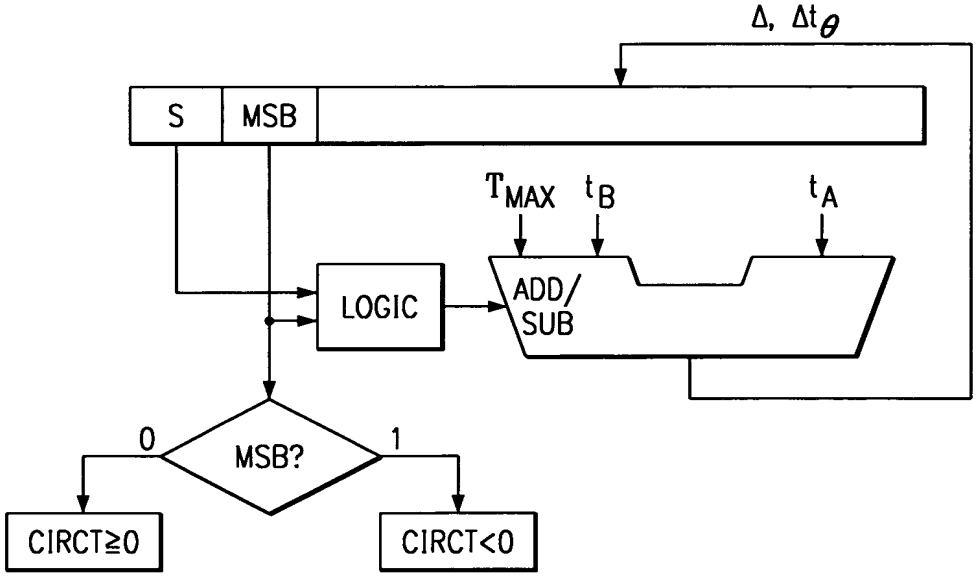

Δ, Δt$_\theta$
S
MSB
T$_{MAX}$
t$_B$
t$_A$
LOGIC
ADD/
SUB
0
MSB?
1
CIRCT≥0
CIRCT<0

FIG. 32

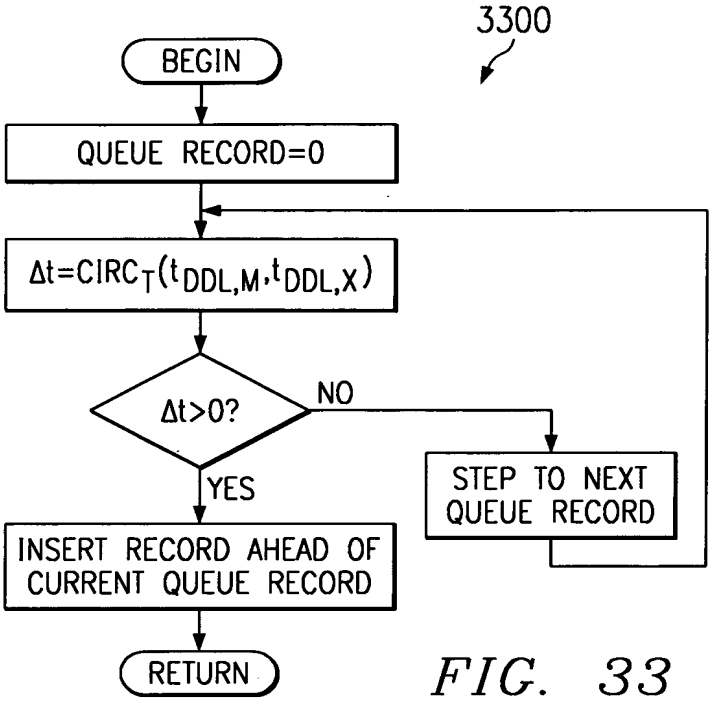


FIG. 33

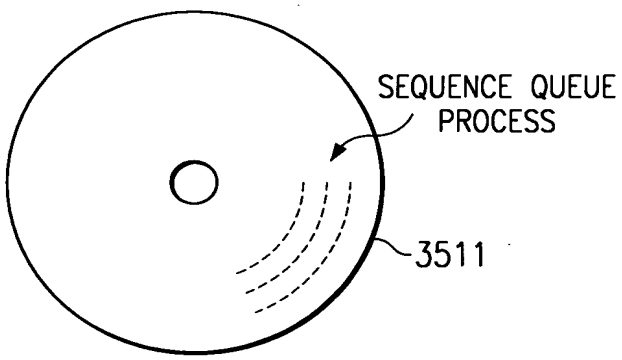


FIG. 35

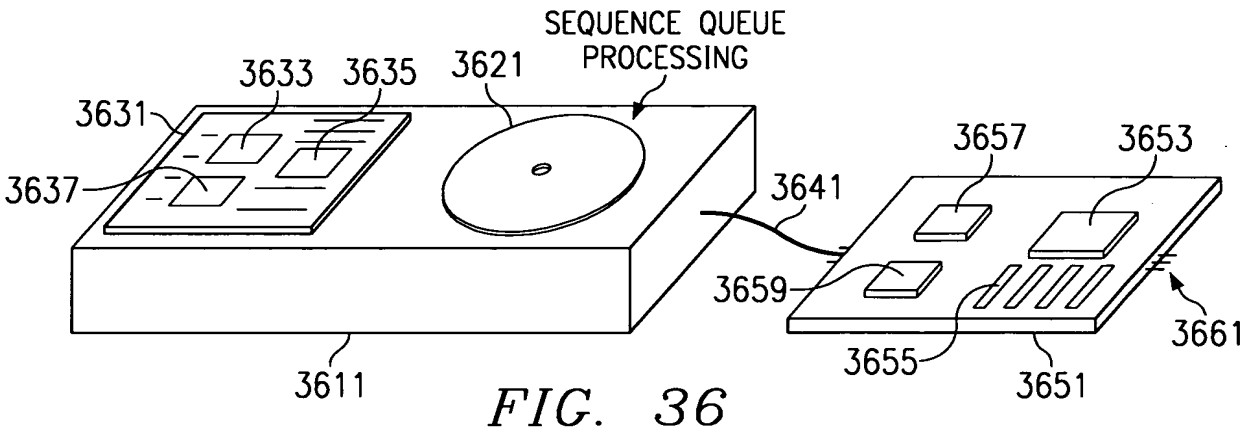


FIG. 36

FIG. 34

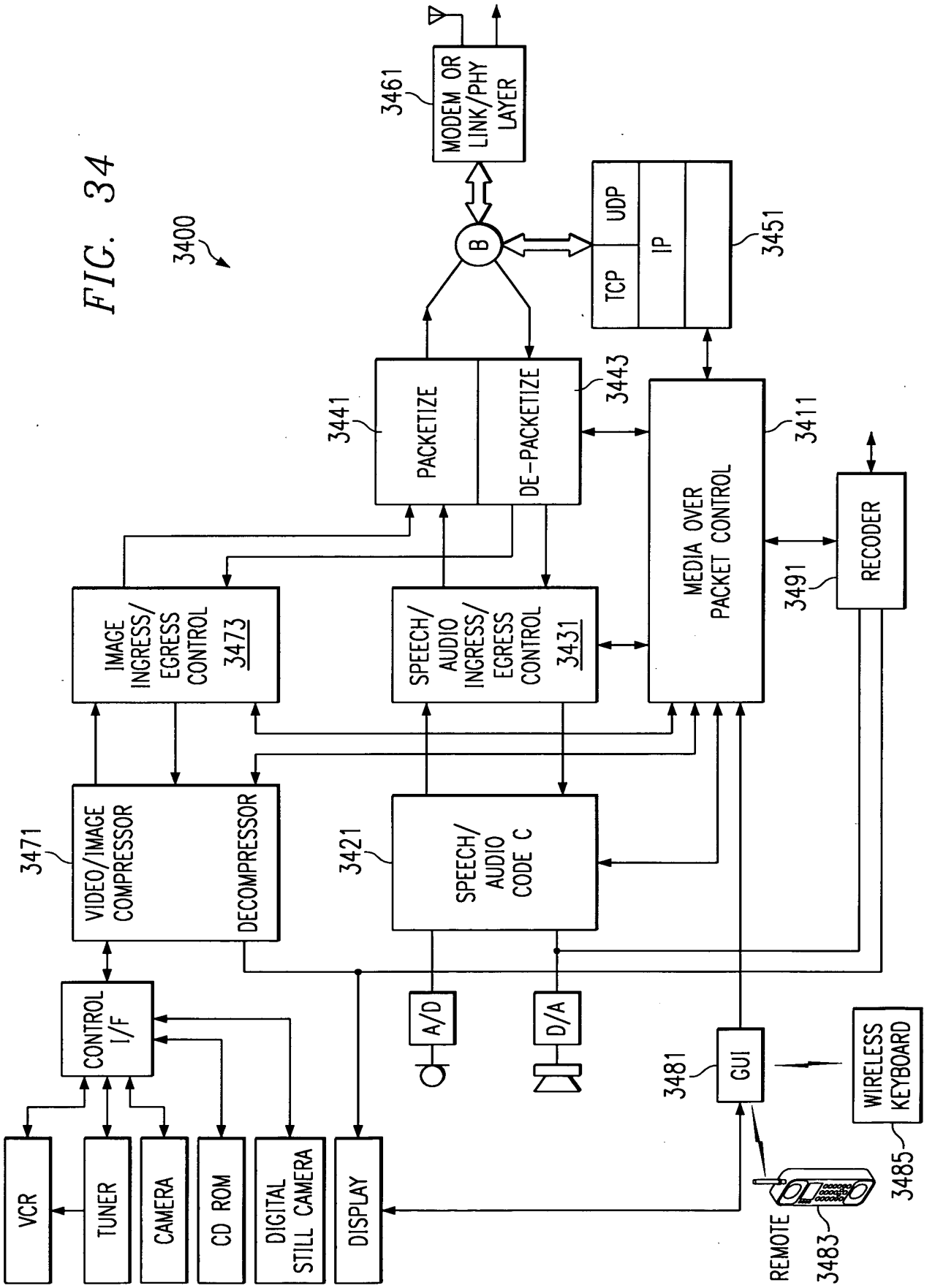

3400
3461
MODEM OR LINK/PHY LAYER
B
UDP
IP
TCP
3451
3441
PACKETIZE
DE-PACKETIZE
3443
3411
MEDIA OVER PACKET CONTROL
3491
RECODER
IMAGE INGRESS/ EGRESS CONTROL 3473
SPEECH/ AUDIO INGRESS/ EGRESS CONTROL 3431
3471
VIDEO/IMAGE COMPRESSOR
DECOMPRESSOR
3421
SPEECH/ AUDIO CODE C
CONTROL I/F
A/D
D/A
3481
GUI
WIRELESS KEYBOARD
3485
VCR
TUNER
CAMERA
CD ROM
DIGITAL STILL CAMERA
DISPLAY
REMOTE
3483

FIG. 37

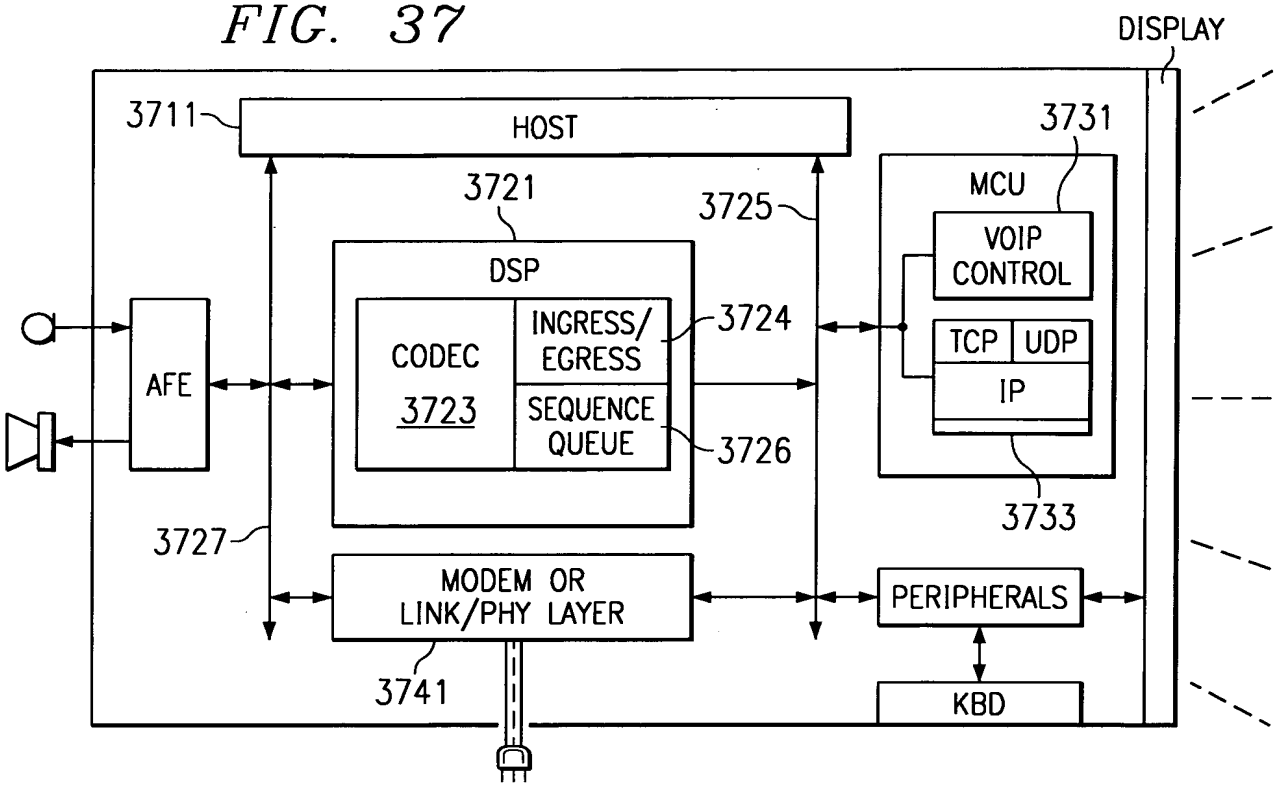
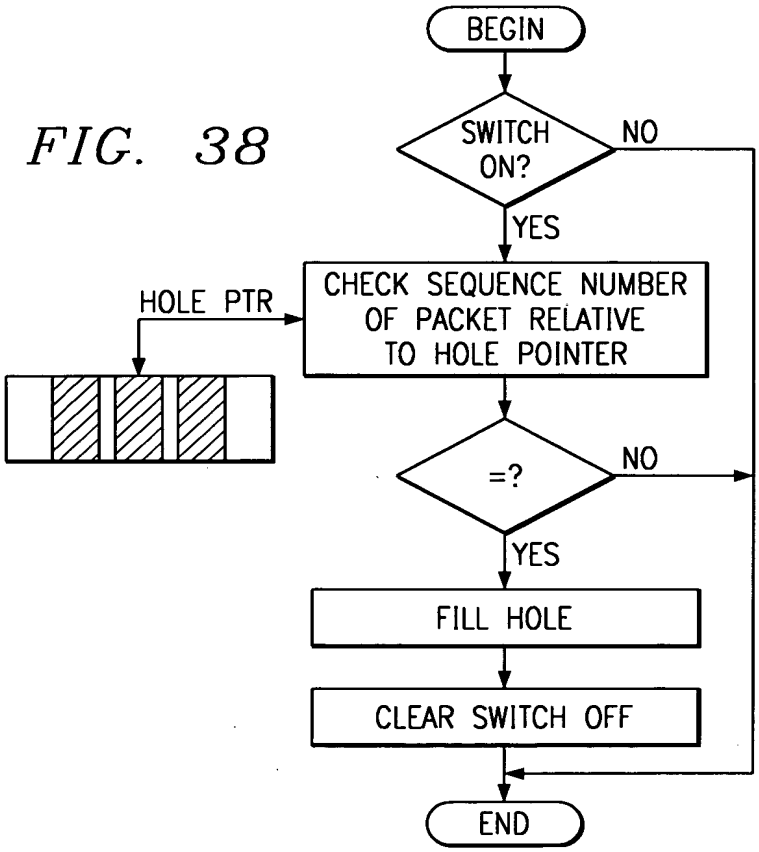

DISPLAY
3711
HOST
3731
MCU
3721
3725
DSP
VOIP CONTROL
AFE
CODEC
3723
INGRESS/ EGRESS
3724
SEQUENCE QUEUE
3726
TCP
UDP
IP
3733
3727
MODEM OR LINK/PHY LAYER
PERIPHERALS
3741
KBD

FIG. 38


BEGIN
SWITCH ON?
NO
YES
HOLE PTR
CHECK SEQUENCE NUMBER OF PACKET RELATIVE TO HOLE POINTER
=?
NO
YES
FILL HOLE
CLEAR SWITCH OFF
END